HITACHI IC MEMORY DATA BOOK



P.O. Box 56310, Pinegowrie 2123 Tel. 789-1400



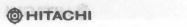
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	* PAC SEINFORMATION	
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	HN462532	
	HN402532	
		Electrically PROM (NMOS)
		AD



	HN462532G	4096-word x 8-bit U.V. Erasable & Electrically PROM (NMOS)
	HN462732	4096-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS)
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280		Electrically PROM (NMOS)
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		Electrically PROM (NMOS)
260	HN482764-4	8192-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS)
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		Electrically PROM (NMOS)
270	HN482764G-3	8192-word x 8-bit U.V. Erasable &
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206	HM10414-1	256-word x 1-bit RAM (ECL 10K)
	HM2110	1024-word x 1-bit RAM (ECL 10K)
	HM2110-1	1024-word x 1-bit RAM (ECL 10K)
300	HM2112	1024-word x 1-bit RAM (ECL 10K)
	HM2112-1	1024-word x 1-bit RAM (ECL 10K)
	HM10422	256-word x 4-bit RAM (ECL 10K)
302		256-word x 4-bit RAM (ECL 10K)
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		HM100422F	256-word x 4-bit RAM (ECL 100K)
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NOTICE

The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied products. The company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.



QUICK REFERENCE GUIDE TO HITACHI IC MEMORIES

	Total	88	100	Organi- zation	Access Time	Cycle Time	Supply Voltage	Power Dissi-		314	Pa	ckag	ge*			Replace-	D
Mode	Bit	Type No.	Process	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	(ns) max	(ns) min	(V)	pation (W)	Pin No.	CC	CG	G	P	FPS	SP	ment	Page
THE	F - 11	HM4334-3	14	IDUI JU	300	460	X BHD	10 /00		11.04	11/2	•	•			HM-6514-9	52
		HM4334-4		CL 1008	450	640	x brie	10µ/20m		100	3 12						52
		HM4334-3L	(0	1001 100	300	460	x bro	10 /00	81	139	0.40	JUI		9			57
	1	HM4334-4L	. (28	ECF 100	450	640	k bnow	$10\mu/20\mathrm{m}$. (SA	13				TETT	57
		HM6148	. (28	EQT 100	70	70	R STIONS	18384		91	84		•			2148	62
		HM6148-6		(1	85	85	t x br	0.1m/0.2			-					2148-6	62
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		HM6148L-6		1024×4	85	85	x bro	$5\mu/0.2$			0	185			7	73117	68
		HM6148H-35**		L. UT	35	35	x bro	1024-w			F-0				1		74
	3	HM6148H-45**		1.17	45	45	a hos	0.1m/0.2			0.0				\forall	2148-45	74
		HM6148H-55**		ur	55	55	x broi	1091-4			-				\forall	2148-55	74
		HM6148HL-35**		(JT	35	35	x han	1024 v			1	131			\forall		78
	4k-bit	HM6148HL-45**		111111111111111111111111111111111111111	45	45	1	$5\mu/0.3$	18		100	06					78
		HM6148HL-55**	100	1.47770	55	55	× bio	1024.w	2 4		200	1					78
		HM6147	35 11	11.77	70	70		- verein			70.6			1	1	2147	83
		HM6147-3	131	1214	55	55	x biol	0.1m/75m			1				1		83
		HM6147L	1.51	CUTT.	70	70					100				1		87
	1	HM6147L-3			55	55		$5\mu/75m$			20	10			\forall		87
		HM6147H-35	- 5 10	LUIT	35	35	x bro	2040	1		12.0			+	\forall	2147H-1	91
		HM6147H-45		4096×1	45	45	x bro	0.1m/0.15			30			1	-	2147H-2	91
		HM6147H-55		. (JTT	55	55	x bron	1024-9			80			1	\forall		91
Static		HM6147HL-35	CMOS	. LITE	35	35	+5	V-9201			명	001		+	+		97
		HM6147HL-45		JTT	45	45	x bron	$5\mu/0.15$		13	88	Ues		++	+		97
	- 6	HM6147HL-55	18 62	CUTT	55	55	x brion	1024-9		1	88	Ods		1	7		97
		HM6116-2		-UTT	120	120	x broi	1024-y							1		101
		HM6116-3		. UTT	150	150	a bron	0.1m/0.18							1		101
	1	HM6116-4		LITT	200	200	or bises	2048-w							7		101
		HM6116L-2	100	LUTT	120	120	x brow	2048-9			on				\forall		124
		HM6116L-3	1300		150	150	-	$20\hat{\mu}/0.16$	15		- N				7		124
		HM6116L-4		via Clusion	200	200	TT eles		Land 1	1000	1007				7		124
	1	HM6116A-10			100	100		110000000000000000000000000000000000000			1	-01		+ +	•		154
		HM6116A-12	610	ock Driv	120	120	I siqu	Quadra		-	- 10	1 853		1	•		154
		HM6116A-15		atovi	150	150	ipia Ed	0.1m/15m		-	E	1345		+-+	0		154
	16k-bit	HM6116A-20		2048×8	200	200			24	-				+-+	•		154
		HM6116AL-10			100	100			-	-				-	•		158
		HM6116AL-12			120	120					-			+ +	•		158
		HM6116AL-15			150	150		5µ/10m		-	-					300	158
		HM6116AL-20	qiupe	tir other	200	200	00 10	riuphia be	ilge	0 1	0	0		1000	•	TT T	158
		HM6117-3	baco	mee a 1	150	150	eg bn	a syllen	tos	W17	1 8	1115				311	-
		HM6117-4	dore	y for any	200	200	on sm	0.1m/0.2	- Vr	001	300	151		•	b	710	162
		HM6117-4		elgmax			descrip	entr prity	aoi	1199	1100	Da	-	-	8.8	1.6	162
					150	150		10µ/0.18		-	-				-		172
		HM6117L-4			200	200											172

(to be continued)



Mode	Total	Type No.	Process	Organi- zation	Access	Cycle	Supply Voltage	Power Dissipa-	D:	W-1-1-20-0	Pac	kage	***	_		Replace-	Page
	Bit		4057	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	(ns) max	(ns) min	(V)	tion (W)	Pin No.	CC	CG	G	P	FP	SP	ment	
		HM6168H-45*	110	CWO	45	45	HdX:									2168	184
		HM6168H-55*	-		55	55		0.1m/0.25	-		5.85	•					184
		HM6168H-70*	82	1000111	70	70											184
294		HM6168HL-45*	24	4096×4	45	45	85-2612		-								185
		HM6168HL-55*			55	55		$5\mu/0.25$			200	(11.7)					185
		HM6168HL-70*	RS. T		70	70	87 1868				83.5	26.14					185
		HM6167			70	70	\$ > 8372	CMOS				•				2167	186
		HM6167-6	83	5/0/0.0	85	85	8> 4888	25m/0.15	-		2.15		•			2167-6	186
	16k-bit	HM6167-8		m2.7	100	100	8×8975		20		a=1					2167-8	186
		HM6167L	88	District.	70	70	5538 × 4	2									192
		HM6167L-6	1 1	54/73s	85	85	2768×8	$5\mu/0.15$			C3.1	1000			1		192
SRAM		HM6167L-8	CMOS	16384×1	100	100	+5	0,470.10		-	108	186					192
	9119	HM6167H-45	188	0.555	45	45	8×8808				•					IMS1400	196
	TNI-92532	HM6167H-55		858. g	55	55	1	0.1m/0.2	-					-	-	11101400	196
		HM6167HL-45	-		_	45	-	-		-			•		-		207
	29.0		- 6	6,738	45		-	$5\mu/0.2$			8.47		•	-	-		+
	12224-2	HM6167HL-55	2.6		55	55	8 15 8 6 6 8	-		1-1	EV.	44	7				207
	7.325	HM6264-10	-	0.788	100	100	-	MINIS	9	1.1	25.14	21.7		-	-		211
	L-ASET	HM6264-12	-		120	120	-	0.1m/0.2		- 1	150	-7	0		-	7 7	211
	64k-bit	HM6264-15	-	8182×8	150	150	8 > 5018		28		1015	-	•	-	-		211
	0.00	HM6264L-10		222.e	100	100		10/0.0			2000	-	•		-		215
	5-7933	HM6264L-12	03	-cer/e	120	120		$10\mu/0.2$	-	-			•	-	_		215
808		HM6264L-15			150	150				1	19.7	1940					215
		HM4716A-1			120	320	+12, +5,		00	3-8	11/8	•	•				222
		HM4716A-2	32	0.354	150	320		20m/0.46	124	1-8	1178		•			MK4116-2	222
		HM4716A-3			200	375	-5,	Zom, c. r.	10	9-8	1175					MK4116-3	222
	16k-bit	HM4716A-4	18	16384×1	250	410	2 v 1002	a Richard			877	•	,•			MK4116-4	222
	TOK-DIC	HM4816A-3	conservation delicated	10004/1	100	235			in land or the contract		Service Co.	•	•			2118-3	233
	- 1	HM4816A-3E			105	200		11m/0.15									233
		HM4816A-4			120	270	6 600 Think	1111/0.13	d pail	Pipe 3	tta S				12	2118-4	233
		HM4816A-7			150	320	in semale	198 110 5	Seated .		12.7%	•	•			2118-7	233
		HM4864-2		BONS	150	270	PENER	20m/0.33	ino.	•	achi		•			150	241
		HM4864-3		THE RESERVE TO	200	335	C 2011/201	20m/0.33	Total Service								241
DDAM		HM4864A-12	NMOS	eason A	120	230			1								260
DRAM	641 14	HM4864A-15	-3	Time	150	260	Boilt	20m/0.275	16	M e						15-14	260
	64k-bit	HM4864A-20		65536×1	200	330	1,710	S Brew J				•	•				260
	2 3	HM4865A-12**	-	XARI	120	230	+5										270
	0 5	HM4865A-15**		120	150	260	1	20m/0.275	- 1	100	100		•				270
	0.0	HM4865A-20**	a a	150	200	330	1		. 3	10,	100						270
	0 0	HM50256-12**		200	120	220	1		- 1	-181	133	•					277
	0 4	HM50256-15**		130	150	260	1	20m/0.35	3-1	.181	1814						277
	0 0	HM50256-20**	10	180	200	330	8	SAUS	P	181	100				1		277
	256k-bit	HM50257-12**	-	262144×1	120	220	1			75	1231	•					284
	- 9	HM50257-15**	1 -	200	150	260		20m/0.35	P.	101	0.014			-	-		284
	9	HM50257-15**	0 -	150	200	330	1	2011/0.33	-	213	138		-	-	-		1
0018		111/130231-20		850	200	330			1	No.	tal						284

MOS ROM-

Page	-soulgabi	Total	Printer and	Dipeipa- tion	Organi- zation	Access	Supply	Power Dissi-	hisar ^o	Pac	kage	***	T	Replace-	Made
Program		Bit	Type No.	Process	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	(ns) max	(V)	pation (W)	Pin No.	С	G	P	FP	ment	Page
184		1.19	HN61364	8K.0\ml.		250	00		28		661				292
		64k-bit	HN61365		8192×8	250	01	$5\mu/0.05$		1	01	•	0.152		294
			HN61366			250	88		24			•	D ASU	17 F F F	296
		128k-bit	HN43128	80/6.25	16384×8 32768×4	6500	70	3 m	28	-	P-1	•	e Mil		298
	Mask		HN613128	CMOS	16384×8	250	+5	$5\mu/0.05$	28	-		•			300
		256k-bit	HN61256	61.9 Vinc	32768×8 65536×4	3500	001	7.5m	28			•	•	16k-bit	302
192			HN613256	31.600	32768×8	250	28	$5\mu/75m$		-	3-	•			304
		1M-bit	HN62301**	l with	131072×8	350	001 1	5m/60m	28		8-		aMi		306
196	15181400	16k-bit	HN462716		2048×8	450	45	0.555	24	•		(11)	10161	2716	310
			HN462532	2.0\m1.		88	55	0.858			•	(15)	aMi	TMS2532	314
			HN462732	\$.0\m2		450	43	0.788		•	•	1973	8161	2732	318
		32k-bit	HN482732A-20	213746	4096×8	200	35		24		•	333	HINE	2732A-2	325
211			HN482732A-25	NMOS		250	100	0.788		-	•	1940	13/8/10	2732A	325
U. V	. Erasable		HN482732A-30	1.1m/0.2		300	120			-	•	100	USHIE CORRE	2732A-3	325
	lectrically		HN482764	-	-	250	+5	8182				1 5	1111	2764	328
215		64k-bit	HN482764-3	5.000	8192×8	300	881	0.555	28			188	tates	2764-3	328
215			HN482764-4	1		450	150					Jaj	81/03		328
		- 1	HN4827128-25**		864	250	851					15.4	1161		332
		128k-bit	HN4827128-30**	NMOS	16384×8	300	150	0.554	28			431	1 Nich		332
			HN4827128-45**	THE LEWIS CO.	8-	450	1198					1.31	à BOE		332
Electri	cally Erasable	16k-bit	HN48016	NMOS	16384×8	350	+5	0.16	24	-	- 2"	•	D PA	-04d-48f	336

^{*} Under development

MOS MEMORIES OF WIDE OPERATING TEMPERATURE RANGE

Mode	Total Bit	Type No.	Organization (word×bit)	Operating Temperature Range	Access Time (ns)	Power Dissipation	Packa	ige**	448	Page
	Dit o	. 0	15	(°C)	max	(W)	Pin No.	P	G	
270		HM6116I-2	20m/ii.225	150 280	120	8821	1.3388 WH			107
		HM6116I-3	2.2.70 /0802	200 230	150	0.1m/0.18	A CHARLES			107
		HM6116I-4		000 001	200	13.60	HMITTH	•		107
	101 14	HM6116LI-2	28 O 1100	-40 to +85	120	99.61	HW MORES	•	•	131
Static RAM	16k-bit	HM6116LI-3	2048×8	200 330	150	20µ4/0.16	24	•	•	131
		HM6116LI-4		120 221	200		HIM BUZES	•		131
		HM6116K-3	30.0\m0S	150 260	150	94.64	PMRME		•	150
284		HM6116K-4		-55 to +125	200	0.1m/0.18	VACARMH	n cesson.	•	150
	THE TE	HM4864I-2			150	M. Louise P. G. Del	nemer Alekset	970		256
D . D.W		HM4864I-3	a sa fullows.	-40 to +85	200	Sex 99 .9 .00		2350		256
Dynamic RAM	64k-bit	HM4864K-2	65536×1	-55 to +85	150	15m/0.3	16	S 84		256
		HM4864K-3		-55 to +85	200					256
EPROM	32k-bit	HN 462732I	4096×8	-40 to +85	450	0.1/0.788	24		•	322

[△] HM6116LPI Series: 10µW



^{**} Preliminary

^{***} The package codes of C, G, P and FP are applied to the package materials as follows.

C: Side-brazed Ceramic DIP, G: Cerdip, P: Plastic DIP, FP: Plastic Flat Package

BIPOLAR RAM

	Total	1530	Organization (word × bit)	Output	Access Time	Supply Voltage	Power Dissipa-	an I	Pack	age**		D 11	Dama
Level	Bit	Type No.		Mot) (3	(ns) max	(V)	tion (mW/bit)	Pin No.	F	G	СС	Replacement	Page
1.13	48,125	HM10414			10		000			•	100	F10414	342
118	256-bit	HM10414-1	256×1	108	8		0.5	1034		•	1	1 /2.01	342
	28134	HM2110			35			10		•		F10415	346
	dates	HM2110-1	1004		25		0.5	16		•		F10415A	346
	41. 1	HM2112	1024×1	000	10		10000	3048	1				350
	1k-bit	HM2112-1			8		0.8			•			350
105	251.80	HM10422	050.44		10		0.8	0.4		•	- 1	F10422	355
ECL 10k	18181	HM10422-7	256×4		7	-5.2	1.0	24				10 50	360
AZB		HM10470		098	25		0/10					F10470	363
		HM10470-1	24		15		0.2	1034					363
		HM10470-15	4096×1	Open	15	or	200	18		•	C 10		368
	4k-bit	HM2142		Emitter	10		0.3				1 1		371
	00131	HM10474	1004344		25		20 00	0.4			150	F10474	374
101	16150	HM10474-15	1024×4	808	15		0.2	24			h		374
o antendered	16k-bit	HM10480	16384×1	consumerably consum	25	THE STREET STREET	0.03	20		•		F10480	379
	11 14	HM100415	1024×1		10		0.6	16				F100415	382
	1k-bit	HM100422	256×4		10		0.8	24		•		F100422	385
	17212	HM100470	4000 × 1		25		0.0	10				F100470	388
ECL 100k	41 1.4	HM100470-15	4096×1		15	-4.5	0.2	18		•			388
100k	4k-bit	HM100474	1001		25		0.0	0.4	•	•		F100474	391
		HM100474-15	1024×4		15		0.2	24		•			391
	16k-bit	HM100480*	16384×1		25		0.05	20		•		F100480	396
	050 1:	HM2504	05011		55					•		93411	399
	256-bit	HM2504-1	256×1		45	1	1.8					93411A	399
		HM2510		Open Collector	70	:1				•			403
TTL		HM2510-1		Conector	45	+5	0.5	16		•		93415	403
	1k-bit	HM2510-2	1024×1		35					•		93415A	403
		HM2511		2	70		0.5			•			407
		HM2511-1		3-state	45		0.5					93425	407

^{*} Preliminary

** The package codes of F, G and CC are applied to the package material as follows.

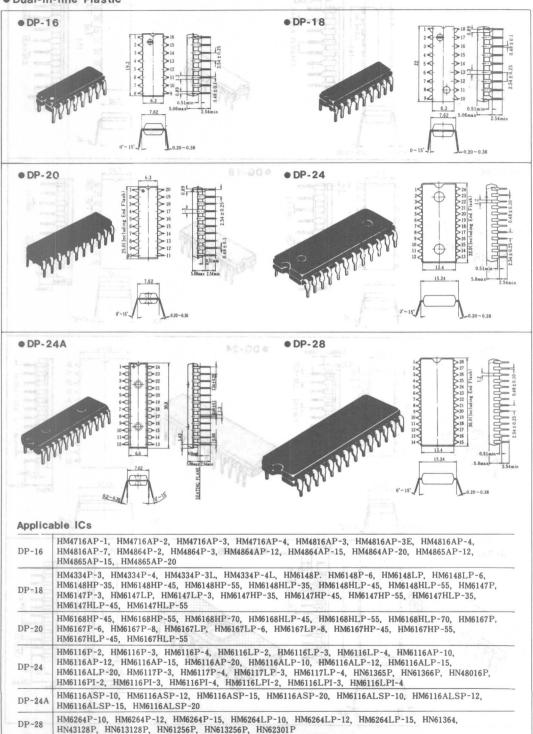
F:Flat Package, G:Cerdip, CC:Side-brazed Ceramic Leadless Chip Carrier

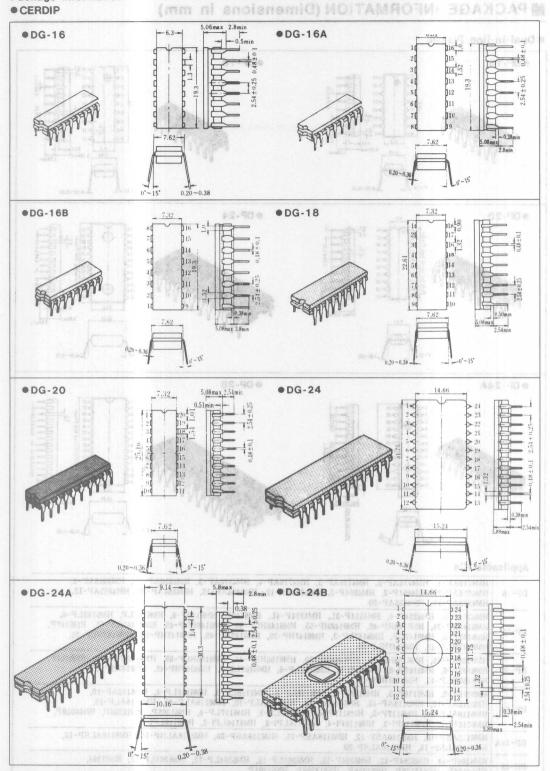
	Total	kage**	Organi- zation	Time Voltag		Supply Voltage						lero'T	
Level	Bit	Type No.	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	Output	(ns) max	(V)	pation (mW)	Pin No.	F	G	P	Replacement	Page
342	11001	HN25044	1004 × 4	0/C	50		500	18			tho	82S136	414
	4k-bit	HN25045	1024×4	3-s	50		500	18	- 1		o ko	82S137	414
	10415	HN25084	ar I	0/C		0					131.2	82S184	419
	A31491	HN25085		3-s	60	8	550	10			27/0	82S185	419
		HN25084S	2048×4	O/C			330	18		•	5170	101.41	422
		HN25085S		3-s	50						5.70		422
355	257012	HN25088	24	0/C			l ix	av.			ijN.	82S180	425
TTL	8k-bit	HN25089		3-s	60	+5		0.00			i Mi	82S181	425
	210170	HN25088S	1004 × 0	0/C	50	8	600	0.4			N lyir	1 11 1	428
		HN25089S	1024×8	3-s	50		Lei	24	1	•	1162		428
		HN25088L		O/C	100		naq()		15	•	Title	11.00	431
		HN25089L		3-s	100	19	350			•	S.Wiz	3 17 11	431
	161 14	HN25168S	2010 × 0	0/C			000	24		•	118	82S190	434
	16k-bit	HN25169S	2048×8	3-s	60		600	24	E 8	•		82S191	434

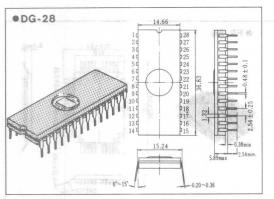
* The	package code of G	is app	olied to	o the i	nateria	l as follows.		23	1×19091	931011	nd-wel	
G:	Cerdip	0										
					MS							
			6									
										ST-0240C (VII)		
									1034×4			
			0									
			0									
			- 00									
			0									
			0									

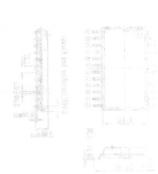
■ PACKAGE INFORMATION (Dimensions in mm)

Dual-in-line Plastic



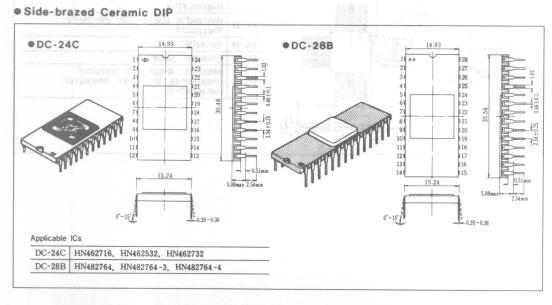




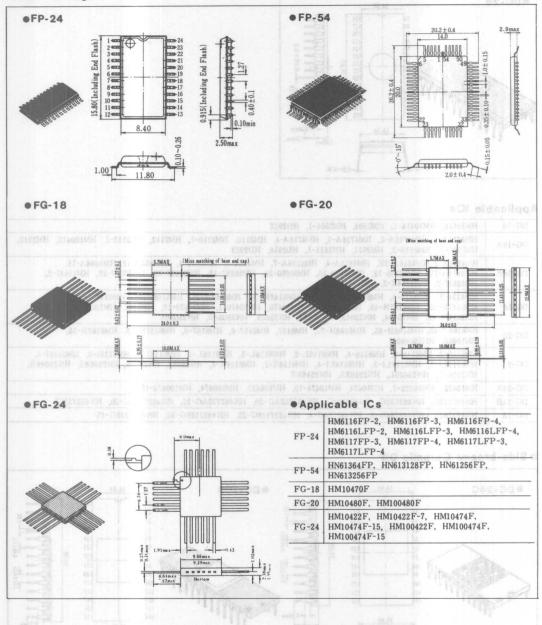


Applicable ICs

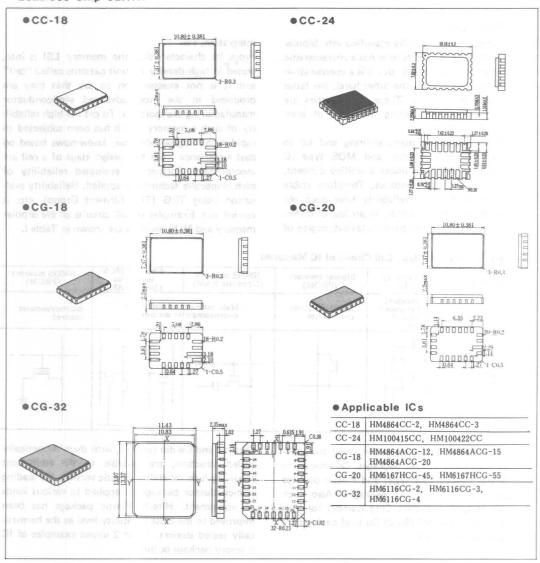
DG-16	HM10414, HM10414-1, HM2504, HM2504-1, HD2912
DG-16A	HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM2110, HM2110-1, HM2112, HM2112-1, HM100415, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923
DG-16B	HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4864-2, HM4864-3, HM4864A-12, HM4864A-15, HM4864A-20, HM50256-12, HM50256-15, HM50256-20, HM50257-12, HM50257-15, HM50257-20, HM4864I-2, HM4864I-3, HM4864K-2, HM4864K-3
DG-18	HM4334-3, HM4334-4, HM6148, HM6148-6, HM6148H-35, HM6148H-45, HM6148H-55, HM6147, HM6147-3, HM6147H-35, HM6147H-45, HM6147H-55, HM10470, HM10470-1, HM10470-15, HM2142, HM100470, HM100470-15, HN25044, HN25045, HN25084, HN25085, HN25084S, HN25085S
DG-20	HM6168H-45, HM6168H-55, HM6168H-70, HM6167, HM6167-6, HM6167-8, HM6167H-45, HM6167H-55, HM10480, HM100480
DG-24	HM6116-2, HM6116-3, HM6116-4, HM6116L-2, HM6116L-3, HM6116L-4, HM6116I-2, HM6116I-3, HM6116I-4, HM6116L-2, HM6116L-3, HM6116LI-4, HM6116K-3, HM6116K-4, HN25088, HN25089, HN25089S, HN25089L, HN25089L, HN25169S
DG-24A	HM10422, HM10422-7, HM10474, HM10474-15, HM100422, HM100474, HM100474-15
DG-24B	HN462716G, HN462532G, HN462732G, HN482732AG-20, HN482732AG-25, HN482732AG-30, HN462732GI
DG-28	HN482764G, HN482764G-3, HN482764G-4, HN4827128G-25, HN4827128G-30, HN4827128G-45



• Flat Packages



• Leadless Chip Carrier





RELIABILITY OF HITACHI IC MEMORIES

1. STRUCTURE

IC memories are structurally classified into bipolar type and MOS type. The former has a characteristic of an extremely high speed. But it is a comparatively small capacity and on the other hand, the latter features a large capacity. These IC memories are utilized by effectively taking the most of their respective characteristics.

Flows from designing, manufacturing and up to inspection for both Bipolar and MOS type IC memories are established under a unified concept, design and inspection standards. Therefore stable results concerning their reliability have been obtained with these IC memories, regardless of differences in the circuit design, pattern, layout, degree of

integration, etc.

From its characteristics, the memory LSI is integrated in high density by unit patterns called "cell" and it is not exaggeration to say that they are produced in the most advanced semiconductor manufacturing technologies. To get the high reliability of such a memory which has been subjected to rapid technological advances, know-hows based on past experience from the design stage of a cell are incorporated. Farther to evaluated reliability of each respective technology applied. Reliability evaluation using TEG (Test Element Group), etc. is carried out. Examples of cell circuits of the Bipolar memory and MOS memory are shown in Table I.

81-DO#

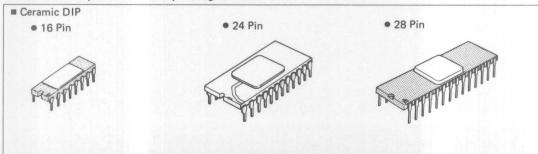
• Table 1 Examples of Basic Cell Circuit of IC Memories

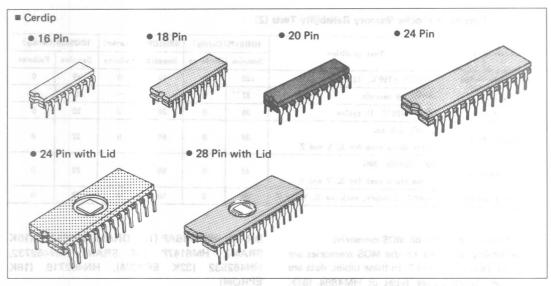
Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory microcompute		For microcomputer control
Example of basic cell circuit					

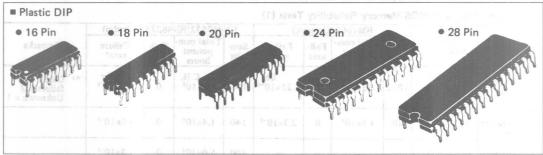
IC memory chips produced in the latest technologies are sealed in different packages. Ceramic package, Cerdip (glass-sealed type) and Plastic package are the current major IC packages. Also such packages as LCC (Leadless Chip Carrier) for high package density and SO (Small Outline) package are now under development.

Ceramic and Cerdip versions, with their hermetically sealed structure, are suitable to the equipment requiring high reliability. Plastic version, the leading semiconductor package, is applied to various kinds of equipment. Hitachi Plastic package has been improved to the close reliability level as the hermetically sealed devices. Table 2 shows examples of IC memory package outlines.

Table 2 Examples of IC Memory Package Outlines







2. RELIABILITY DATA Results of reliability tests are listed below.

2-1 Reliability test data on Bipolar memories

The reliability test data on the Bipolar memories are shown in Tables 3 and 4. Since they are manufactured under the aforementioned standardized design

rules and quality control, there is no difference in reliability among various types. In addition, it can be said that the greater the capacity, the higher the reliability per bit.

• Table 3 Results on Bipolar Memory Reliability Tests (1)

ENTERIOR S	Petr	815	HM10470	(Cerdi	ip)	87	HM100422(Chip Ca	rrier)	-	HN25089	(Cerdi	p)
Test item	Test condition	sam-	Total component hours	Fail- ures	Failure rate*	Sam-	Total component hours	Fail- ures	Failure	Sam-	Total component hours	Fail- ures	Failure
i wagaatani i wagaatani	Ta=125°C		0.11										
A LANCE TO SERVE	$V_{EE} = -5.2 \text{V} (\text{HM}_{10470})$	1	С. Н.	+	1/hr						C. H.		1/hr
High-	$V_{cc} = 5.5 \text{V} (\text{HN25089})$	125	4.0×10 ⁵	0	2.3×10 ⁻⁶	2.0		Hist	45 1	36	3.6×10 ⁴	0	2.6×10 ⁻⁶
temperature (Operating)	$T_a = 150 \text{ °C}$ $V_{EE} = -5.2 \text{ V (HM10470)}$ $V_{EE} = -5.0 \text{ V (HM100422)}$ $V_{cc} = 5.5 \text{ V }$ $t_{tyre} = 1 \mu_{\text{S}}$ (HN25089)	80	2.7×10 ⁵	0	3.4×10 ⁻⁶	40	4×10 ⁴	0	2.3×10 ⁻⁵	10	1.0×10 ⁴	0	9.2×10 ⁻⁵
High-	Ta=200 °C	27	2.7×10 ⁵	0	3.4×10 ⁻⁵	40	4×10 ⁴	0		15	1.5104		0.110-5
temperature		-		U		40	4 ^ 10	0	2.3×10 ⁻⁵	15	1.5×10 ⁴	0	6.1×10 ⁻⁵
storage	Ta = 295 °C	20	2.0×10 ⁵	0	4.6×10 ⁻⁵	40	4×104	0	2.3×10 ⁻⁵	15	1.5×104	0	6.1×10 ⁻⁵

^{*} Estimated failure rate with confidence level $60\,\%$



• Table 4 Results on Bipolar Memory Reliability Tests (2)

100		HM10470	(Cerdip)	HM100422(C	Chip carrier)	HN25089(Cerdip)	
Test item	Test condition	Samples	Failures	Samples	Failures	Samples	Failures
Temperature cycling	-65 °C∼+150 °C, 10 cycles	120	0	40	0	45	0
Soldering heat	260 °C, 10 seconds	22	0	K #3	-	22	0
Thermal shock	0°C~+100°C, 10 cycles	36	0	20	0	22	0
Mechanical shock	1500G, 0.5 ms, Three times each for X, Y and Z	30	0	60	0	22	0
Variable frequency	100~2000Hz, 20G Three times each for X, Y and Z	40	0	60	0	22	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	60	0	22	0

2-2 Reliability test data on MOS memories

The reliability test data on the MOS memories are shown in Tables 5, 6 and 7. In these tables, data are shown on representative types of HM4864 (64K

DRAM), HM4716AP (16K DRAM), HM6116P (16K SRAM), HM6147P (4K SRAM), HN462732, HN462532 (32K EPROM), HN462716 (16K EPROM)

• Table 5 Results on MOS Memory Reliability Tests (1)

PROTESTA		-351)	HM4864	(Ceran	nic)	HN	1462532/HN	46273	2 (Cerdip)	# 15 Pln
Test item	Test condition	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Remarks
High- temperature dynamic operation	Ta=125°C V _{CC} =5.5V t _{cyc} =3 μs	1872	C.H. 3.33×10 ⁶	3*1	1/hr 1.25×10 ⁻⁶	100	C.H. 1.0×10 ⁵	0	1/hr 9.2×10 ⁻⁶	*1 Oxide failure × 2 Unknown × 1
High- temperature, storage	Ta=200° C	20	4.0×10 ⁴	0	2.3×10 ⁻⁵	140	1.4×10 ⁵	0	6.6×10 ⁻⁶	
High- temperature storage	Ta=259°C	-	-			100	5.0×10 ⁴	0	1.8×10 ⁻⁵	LINE AND LONG OF
High- temperature storage	Ta=295°C	- Ja	quality oq	bns :	elus —	100	4.2×10 ⁴	1*2	4.8×10 ⁻⁵	*2 Data disappearance

^{*} Estimated failure rate with confidence level 60%

• Table 6 Results on MOS Memory Reliability Tests (2)

			HM4716A	P (Plas	stic)	Н	M6116P/HM	16147P	(Plastic)	A
Test item	Test condition	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Remarks
High- temperature dynamic operation	Ta=125°C VDD=13.2V (NMOS) VCC=5.5V (CMOS) t _{cyc} =3μs	2330	C.H. 3.46×10 ⁶	6*1	l/hr 2.12×10 ⁻⁶	1216	C.H. 1.90×10 ⁻⁶	3*2	l/hr 2.19×10 ⁻⁶	*1 Oxide failure × 6 *2 Oxide failure × 1 Electrostatic discharge × 1 Unknown × 1
High- temperature storage	Ta=150°C	45	4.5×10 ⁴	0	2.0×10 ⁻⁵	20	2.0×10 ⁴	0	4.6×10 ⁻⁵	F = 35 V
High- temperature and high- humidity bias	Ta=85°C, RH=85% VDD=12V (NMOS) VCC=5.5V (CMOS)	3081	6.2×10 ⁶	19*3	3.1×10 ⁻⁶	630	1.3×10 ⁶	4*4	4.0×10 ⁻⁶	*3 Aluminium corrosion x 17 Unknown x 2 *4 Aluminium corrosion x 3 Unknown x 1

^{*} Estimated failure rate with confidence level 60%.

Table 7 Results on MOS Memory Reliability Tests (3)

Test item	Tast andition		1864 mic)	HM4 (Cer	1864 dip)		ROM rdip)	HM47	16AP	HM6 HM6	147P
Test item	Test condition	Sam- ples	Fail- ures								
Temperature cycling	-65°C~RT~150°C 10 cycles	1208	0	260	0	50	0	-	-	_	_
Temperature cycling	-55°C~RT~150°C 10 cycles	_	-	-	-	310	0	7892	0	2080	0
Temperature cycling	-55°C ~ 150°C 1000 cycles	164	0	100	0	50	0	600	0	_	-
Thermal shock	-65°C ~ 150°C 15 cycles	22	0	60	0	72	0	190	0	_	_
Thermal shock	0°C ~ 100°C 15 cycles	_	_			197	0	138	0	60	0
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	128	0	60	0
Mechanical shock	1,500G, 0.5ms	22	0	38	0	38	0	, î -	-	-	_
Variable frequency	20~2,000Hz, 20G	22	0	38	0	38	0	_	_	_	-
Constant- acceleration	20,000G	22	0	38	0	38	-0	-	_	_	-

2.3 Change of electrical characteristics under endurance test for IC memories

The degradation of ICBO of the cell transistor, degradation of hFE, etc., can be considered as main factors in the internal elements for reliability of Bipolar memories. In actual element designing, however, it has been designed to operate in the range at which these degradations do not happen. Therefore changes of electrical characteristics including access time are not observed.

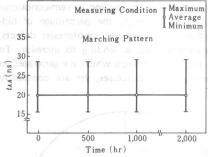
Time dependence in access time for HM10470 is shown in Fig. 1.

Fig. 1 Example of Change in Bipolar Memory Characteristics

and pairmofted bEx	ample org seeks privation	Exampl
Device name	нм 10470 — разлеча	\ \text{\tin}\text{\ti}\\\ \text{\text{\text{\text{\text{\text{\text{\text{\text{\texi}\text{\texi}\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\ti}\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\ti}\text{\text{\text{\text{\text{\text{\text{\text{\ti}\ti}\\\ \tittt{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\ti}}\\ \tittt{\text{\text{\text{\text{\texi}\text{\text{\texi}\til\tittt{\text{\ti}\tintti}\tittt{\text{\ti}\tittt{\text{\ti}\tinttit{\text{\texi}\ti
Test condition	$Ta=125^{\circ}C, V_{EE}=-5.2V$	10
Failure criteria	$t_{AA} = 25 \text{ns}$	die
Failure mechanism	Surface degradation	15, 70
Pesults:	I A	1

Access time (tAA) is stabilized and is within the failure criteria.

le of time change in access time for Bipolar memory Maximum Measuring Condition Average



V_{TH} is a basic parameter in the MOS memories, however, it has been confirmed there is not any shift in V_{TH} for practical usage because we have applied surface stabilizing technique, clean process, etc.

In case of dynamic RAM which needs refresh cycle. refresh time is also stabilized owing to the abovementioned process. Time dependence of Vcc min and t_{REF} characteristics for the 64K DRAM are shown in Fig. 2 and 3.

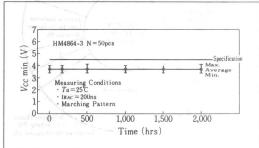
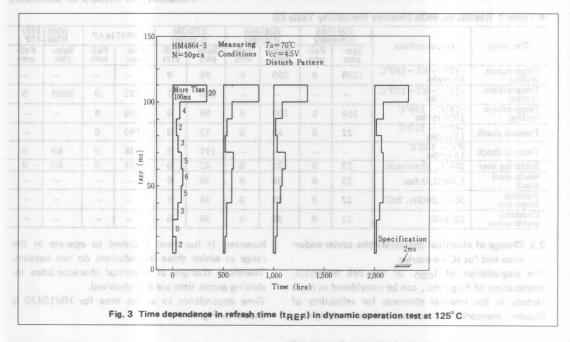


Fig. 2 V_{CC} min time dependence in dynamic operation test at 125° C



2.4 Classification of failure modes

Examples of failures happened in the field are shown in Fig. 4 and 5. Since memory LSIs generally require the most fine processing in semiconductor manufacturing technology, the percentage of failures resulting from pinholes, photoresist defects, foreign materials, etc., is tending to increase. To eliminate the latent defects which are generated in these manufacturing processes, we are constantly

improving these processes, and performing burn-in screening under high temperature for all memories. In addition, since the analysis of failures in the field can result in important feedback to improve their design and manufacturing, we are always exerting our efforts to collect customer process data and field data with the aim of further establishing their high reliability.

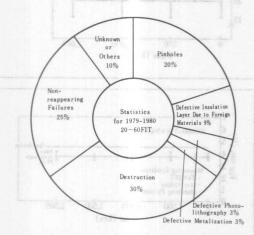


Fig. 4 Classification of Failure Modes of Bipolar Memory in the field

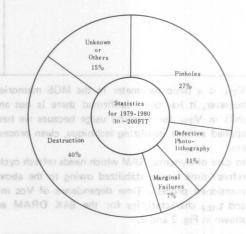


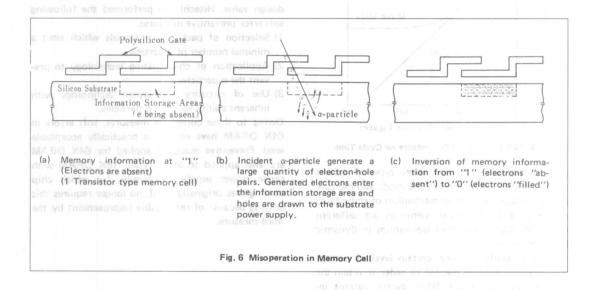
Fig. 5 Classification of Failure Modes of MOS Memory in the field

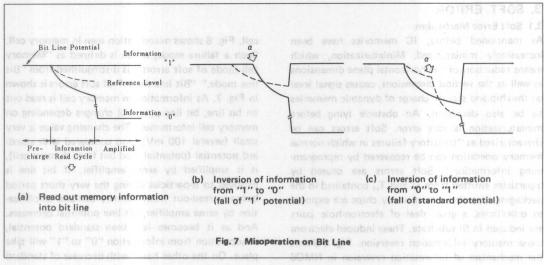
3. SOFT ERROR

3.1 Soft Error Mechanism

As mentioned before, IC memories have been increasingly miniaturized, Miniaturization, which means reduction of the horizontal plane dimensions as well as the vertical dimensions, causes signal level on the chip and storage charge of dynamic memories to be also decreased. An obstacle lying before miniaturization is soft error. Soft errors can be characterized as "transitory failures in which normal memory operation can be recovered by reprogramming information." Soft errors are caused by α-particles emitted from U and TH contained in the packaging materials. As memory chips are exposed to α-particles, a great deal of electron-hole pairs are induced in Si substrate. These induced electrons cause memory information reversion. Fig. 6 shows the mechanism of information reversion in NMOS dynamic memory by α -particles. In case of NMOS dynamic memory, negative voltage is applied to the Si substrate. Therefore, positive holes are drawn by substrate, and only electrons cause information reversion (from information "1" to "0") of memory

cell. Fig. 6 shows misoperation seen in memory cell. Such a failure mode, which is defined as "Memory cell mode of soft errors," is distinguished from "Bit line mode." "Bit line mode" of soft errors is shown in Fig. 7. As information in memory cell is read out on bit line, bit line potential changes depending on memory cell information. The changing value is very small (several 100 mV), and compared with standard potential (potential read out from dummy cell). it is amplified by sense amplifier. If bit line is exposed to α-particles during the very short period between read-out from memory cell and amplification by sense amplifier, bit line potential decreases. And as it becomes less than standard potential. misoperation from information "0" to "1" will take place. On the other hand, with decrease of standard potential, misoperation from information "1" to "O" is seen. Both are called "Bit line mode" because errors appear at irradiation of α -particles. Soft error dependence on cycle time is shown in Fig. 8.





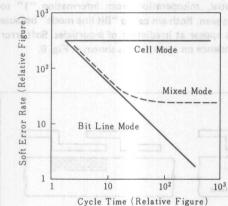


Fig. 8 Soft Error Rate's Dependence on Cycle Time

Actual products will have three types of failure modes, that is, cell mode, bit line mode and mixture of both modes. Soft error mechanism of static MOS memories and of bipolar memories are different from the above-mentioned mechanism in dynamic MOS memories.

In case of static memory, certain level of current always flows through the cell in order to retain the data in flip-flop circuit. When partial current induced by α -particles exceeds the retention current, misoperation occurs because of reversion of flip-flop circuit.

3.2 Examples of soft error preventive measures in products

At the initial stage of the 64K DRAM development, its soft error rate was estimated from accelerated irradiation test data to be higher than the expected design value. Hitachi has performed the following soft error preventive measures.

- 1) Selection of packaging materials which emit a minimal number of α -particles.
- Application of chip coating technology to prevent the α-particles.
- 3) Use of circuitry and layout technology with inherent ability to resist α -particles.

Owing to these corrective measures, soft errors in 64K DRAM have reached a practically acceptable level. Preventive measures applied for 64K DRAM are also applied to other types. 16K DRAM with single power supply 5V family, for which chip coating was originally used, no longer requires this coating because of remarkable improvement by the third measure.

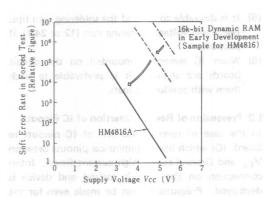


Fig. 9 Example of Soft Error Improvement on 16K-bit

Dynamic RAM

3.3 Request for soft error preventative measures in

Thus our efforts to reduce soft errors have resulted in almost trouble-free memories. System reliability can be more improved by supplying some functions, that is, ECC device for lage memory system and parity bit for small one.

Voltage influeed at an envoir detroys (Cs. Mount and remove IC are supply voltage is out onto Same precaution at he marks in measurement with rester.

L bipolar mainory sign cut off frequency of nestor. Therefore sarrefimes, logoillation is used in relation with the remail directly, and misoperion of ICs is denue. It such cases, about 0.1 of capacitor with the good high frequency architectures, is necessarily mison.

1.5 Preception on . ple "H" Level of ECL

cases, it is see "hat input of ICs is directly to ground for input as "H" level of the control of the input as "H" level with internal articommosition, "H" and el of input a postified as Villiam) and of input a curely. Please refer them

Coding over dissipation of solar memory is 400mW to 000mW depending or voduces. In the case manipolar memories are suited on she board, natural covertion is insufficient to cooling. Therefore leaver non-forced, at a district with videors block.

4. RELIABILITY CLASSIFICATION

In designing IC memories, Hitachi classifies memory reliability by their application and controls the flows of design, production and test. Reliability can be roughly classified as follows:

- (I) For large scale computers and electronic exchangers
- (II) For important parts for auto-motive application
- (III) General communication-industrial use In using our products, therefore, we would like you to consider the classification of the application. Especially, when you are going to apply our memories to any special equipment, please do not hesitate to consult our sales engineering staff.

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A variety of IC memories of high-spped, high-power and static lower power dissipation CMOS have been developed and commercially available, which allows an electronics designer to properly select the one best suited for a particular application. However, he must be familiar with the advantages and disadvantages of the devices to make the optimum selection and to prevent them from malfunctioning or, in the worst case, from breaking down. Precautions for handling IC memories given below will help the electronics designers to work out their optimum circuit designs.

1. BIPOLAR IC MEMORY

1.1 Prevention of static electricity

Bipolar memories have been considered to have high resistance to the static electricity than MOS ICs. However, the presently available high speed IC, represented by bipolar memories, must be provided with a suitable preventive measure against the static electricity. Because their diffused junctions have become thinner than the conventional types, in order to perform higher capability. Take note of the following points.

- (1) Keep all terminals of a device in the conductive mat during transportation and storage to keep them at the same potential. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specially stated, all HITACHI IC memories will be shipped in our conductive mats. Store them as they are.
- (2) When handling by hand IC memories for inspection or connection, his finger must be grounded as shown in Fig. 1. Do not forget to insert a 1M ohm resistor to protect him against an electric shock.

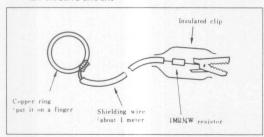


Fig. 1

- (3) It is advisable to control the ambient relative humidity at about 50 per cent to prevent the occurrence of static electricity.
- (4) It is also recommendable to wear cotton clothes instead of the ones made of synthetic fabrics to prevent the static electricity from occurring.

- (5) It is desirable to ground the soldering iron tips. Use a low voltage soldering iron (12 or 24V), if possible.
- (6) When IC memories mounted on the circuit boards are shipped, it is preferable to pack them with conductive mats.

1.2 Prevention of Reverse Insertion of IC Pinouts

In the case of reverse insertion of IC pinouts to board, ICs which have symmetrical pinouts between VEE and Ground causes high current flown. Interconnection on the chip is melted and device is destroyed. Precaution must be made even for the ICs which do not have symmetrical pinouts between VEE and Ground, because excess current flows and sometimes device is destroyed. On the device package, marking of No. 1 pin is stamped. Please watch this marking and insert ICs properly.

1.3 Mounting and Removal of ICs during Voltage is supplied

Usually, rather high current flows in regulator of bipolar memory. Therefore, if ICs are put in and pulled out to board during voltage is supplied, high voltage induced at current on/off destroys ICs. Mount and remove ICs after supply voltage is cut off. Same precaution must be made in measurement with tester.

1.4 Prevention of Oscillation

ECL bipolar memory has high cut-off frequency of transistor. Therefore, sometimes, oscillation is caused in relation with external circuit, and misoperation of ICs is occurred. In such cases, about 0.1 μF of capacitor, which has good high frequency characteristics, is recommended to put between ICs and voltage supply line.

1.5 Precaution on Simple "H" Level of ECL Memory

In some cases, it is seen that input of ICs is directly connected to ground to fix input as "H" level. However, it sometimes causes misoperation in conjunction with internal circuit composition. "H" and "L" level of input are specified as $V_{\rm IL\,(min)}$ and $V_{\rm IH\,(max)}$ for ICs respectively. Please refer them and use ICs properly.

1.6 Cooling

Power dissipation of bipolar memory is 400mW to 1000mW depending on products. In the case many bipolar memories are mounted on the board, natural convention is insufficient for cooling. Therefore, please run forced air cooling with velocity higher

than 2.5m/s. In addition, by cooling, improvement of reliability can be expected as shown in Fig. 2. We recommend the junction temperature to be kept less than 85°C for high reliability use.

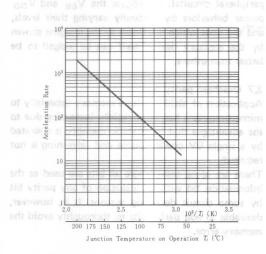


Fig. 2 Example of derating of ECL

1.7 Other Precautions

(1) Deforming of magazine and carrier

Since material of plastic magazine and carrier (for ECL flat package) is usually thermal plasticity, they deforms at temperature higher than 40 to 50°C and may not perform sufficiently. If burn-in is carried out at users, please use aluminum magazine or other metal fixtures.

(2) Shock at transportation

Glass sealed type package is fragile. Usual handling and drop test (JIS C7021 A-8) on individual devices do not cause any problem. However, it devices packed in magazine receive strong shock such as drop shock, devices hit neighbouring devices and packages may be damaged. Therefore, at transportation or loading on/off, be careful not to drop them. Even after devices are mounted on board, IC packages may be damaged if strength of board is not enough and board receives strong deforming stress. Please be careful on strength of board and handling. If any questions rose at using Hitachi products, please feel free to contact closest Hitachi representatives or offices.

2. MOS IC MEMORY

2.1 Prevention of static electricity

Similar to bipolar IC memories, suitable preventive measures should be taken for MOS IC memories by referring to paragraph 1.1.

2.2 Absorption of power source noise

The source current level flowing in the dynamic memory during the time of access is considerably different from that of stand by. Although the current difference is quite effective to save the power consumption, the current spike may be developed into the power source noise. Since all MOS IC memories are, in general, accessed while being refreshed, it is recommended to insert large capacitors (a 10 μ F capacitor for every 9 pieces of 16K-bit HM4716A, for example) as well as a 0.1 μ F capacitor having good high-frequency characteristics for each memory. Needless to say, it is very important to reduce the power circuit impedance when designing.

2.3 Current spike in VBB power

The V_{BB} power is necessary for maintaining the IC memory function in the reverse bias and the current does not generally exceed the level of the reverse leakage current. However, in order to prevent an accidental current spike which is sharply formed in either positive or negative phase by the rise or fall clock pulse at the time of access, use a 0.1 μ F capacitor for every 2 or 3 memories for absorbing such noises.

2.4 Clock drive ICs

The TTL to MOS clock drive ICs have special designs so that they are capable of quick increase in the capacitive load. If a ground wire short-circuits either $V_{\rm DD}$ or $V_{\rm CC}$ which appear in the Pin No. 1 and No. 16 respectively, when the device is at high level, the device may be broken down. Carefully eliminate such possibility beforehand.

2.5 Power application sequence

It is advisable to design the circuits so that power is applied in the sequence of V_{BB} , V_{DD} and V_{CC} and interrupted in the reverse sequence, here the reverse bias V_{BB} is applied first and interrupted last.

It may be impossible for some small-scaled systems to apply power in the above-mentioned sequence (for example, when the V_{BB} is supplied by a DC to DC converter). According to our experiments conducted in the under-mentioned test conditions, it



has been proved that such a small-scaled system as to consist of 200 to 300 memory devices is not affected by he power application sequence.

Power application sequence test for N MOS IC

- 1.) Test method
- (1) Ambient temperature: 25°C
- (2) Power voltage: V_{DD}=13.2V, V_{CC}=5.0V,

The source curred VIH=5.0V THE dynamic

(3) Operation mode: AC operation ("0" to

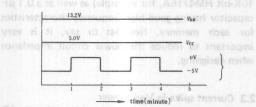
"16383" all bits scanning).

ent eval of training tour = 10 µs margin to the the

Read modify write operdeveloped into the po nois source noise. Since all

(4) V_{BB} power: ON (1 min.) – Floating

being refreshed, it (.nim 1) mended to insert large



2.) Test results

Type No.	Number of cycles	Number of sample	Number of failures
HM4716A	2000 cycles	50	0

2.5 Power application secuence

2.6 Assessment of the memory system design

It is quite effective to obtain the power margin curves (shmoo curve) for evaluating the memory system designs (timing margin or adaptability to the peripheral circuits). Investigate the VBB and VDD power behaviors by gradually varying their levels, and the ones which are closer to the margine shown by the memory device itself can be judged to be better than others.

2.7 Overhead parity bit

Application of MOS IC static memory especially to microcomputers has been rapidly increasing due to the advantages that MOS static memory is operated by a single 5V power source and refreshing is not required.

There are some cases where all bits are used as the information bit without inclusion of any parity bit by some circuit designing reasons. It is, however, desirable to add parity bits to thoroughly avoid the memory error.

Glass sealed to be paukage is fragile. Usual

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual users' purchase purpose and quality reguired, and to be at the satisfied quality level considering general marketability. Quality reuired by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize the quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality. In addition, quality required by users on semiconductor devices are going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

- Build the reliability in design at the stage of new product development.
- (2) Build the quality at the sources of manufacturing process.
- Execute harder the inspection and reliability confirmation of final products.
- (4) Make quality level higher with field data feed back.
- Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as wel as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition.

failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely sude and execution of design standardization, device design (include process

design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishement of design rule, and standerdization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

- 1. Purposes of Test Site are as follows;
 - Making clear about fundamental failure mode
 - Analysis of relation between failure mode and manufacturing process condition
 - Search for failure mechanism analysis
 - Establishment of QC point in manufacturing
- 2 Effectiveness of evaluation by Test Site are as follows:
 - Common fundamental failure mode and failure mechanism in devices can be evaluated.
 - Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
 - Able to analyze relation between failure causes and manufacturing factors.
 - · Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competition power of products, the major purpose of design review is to insure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even

for design changed products. Items discussed and determined at design review are as follows;

- Description of the products based on specified design documents.
- (2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub program of calculation, experiments, investigation, etc. will be carried out.
- Determine contents of reliability and methods, etc. based on design document and drawing.
- (4) Check process ability of manufacturing line to achieve design goal.
- (5) Discussion about preparation for production.
- (6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
- (7) Reference of past failure experiences with similar devices, confirmation of method to provent them, and planning and execution of test program for confirmation of them. These study and decision are made using check lists made individually depending on the objects.

from the planning stage inn new products and even

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

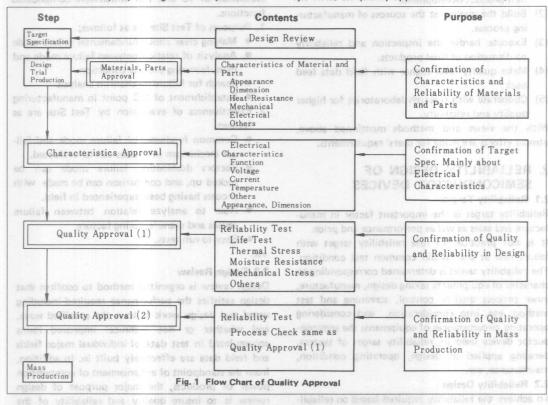
- (1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
- (2) Feedback of information should be made to insure satisfied level of process ability.
- (3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To insure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

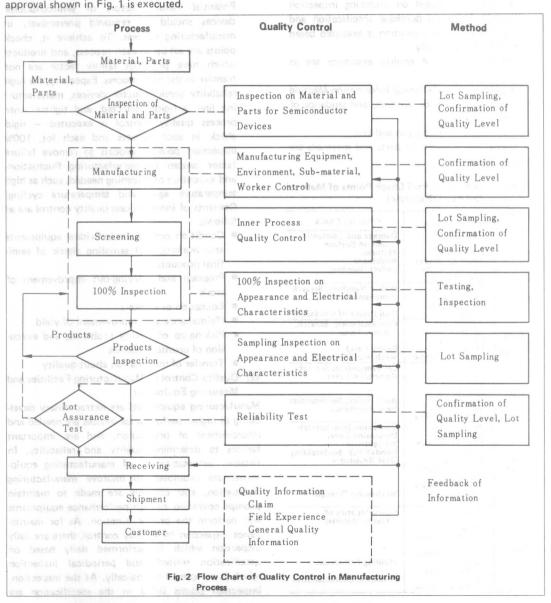
The views on quality approval are as follows;



- (1) The third party executes approval objectively from the stand point of customers.
- (2) Fully consider past failure experiences and information from field.
- (3) Approval is needed for design change and work change.
- (4) Intensive approval is executed on parts material and process.
- (5) Study process ability and fluctuation factor, and set up control points at mass production. Considering the views mentioned above, quality approval shown in Fig. 1 is executed.

3.3 Quality and Reliability Control at Mass Produc-

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.



3.3.1 Quality Control of Parts and Material

As tendency toward higher performance and higher reliability of semiconductor devices, is going, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows:

- (1) Outside Vendor Technical Information Meeting
- (2) Approval on outside vendors, and guidance of outside vendors
- (3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance Dimension Sheet Resistance Defect Density Crystal Axis	Damage and Contamina- tion on Surface Flatness Resistance Defect Numbers
Mask	Appearance Dimension Resistoration Gradation	Defect Numbers, Scratch Dimension Level Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance Dimension Purity Elongation Ratio	Contamination, Scratch, Bend, Twist Purity Level Mechanical Strength
Frame	Appearance Dimension Processing Accuracy Plating Mounting Characteristics	Contamination, Scratch Dimension Level Bondability, Solderability Heat Resistance
Ceramic Package	Appearance Dimension Leak Resistance Plating Mounting Characteristics Electrical Characteristics Mechanical Strength	Contamination, Scratch Dimension Level Airtightness Bondability, Solderability Heat Resistance
Plastic	Composition Electrical Characteristics Thermal Characteristics Molding Performance Mounting Characteristics	Characteristics of Plastic Material Molding Performance Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub materials. The manufacturing inner process quality control is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and tighter inner process quality control is executed - rigid check in each process and each lot, 100% inspection pointed process to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures
- Transfer of information about quality
- (2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipments are extraordinary developing as higher performance devices are needed and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain prompt operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are

checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances – temperature, humidity, dust – and the control of

submaterials — gas, pure water — used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

1	Process	Contr	ol Point	Purpose of Control
,	Purchase of Material		Tameste	
Wafer-]	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
	Surface Oxidation	Oxidation		Assurance of Resistance
	Inspection on Surface Oxidation		Appearance, Thickness of Solad Oxide Film	Pinhole, Scratch
	Photo Resist	Photo Resist		J
	□ Inspection on Photo Resist ○ PQC Level Check	Resist	Dimension, Appearance	Dimension Level Check of Photo Resist
	Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
	Inspection on Diffusion	8	Gate Width	Control of Basic Parameters
	◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	(VTH, etc) Cleaness of surface Prior Check of VIH Breakdown Voltage Check
	Evaporation	Evapo- ration	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
	○ Inspection on Evaporation ○ PQC Level Check		, wy ngi sad	
	Wafer Inspection	Wafer	Thickness, VTH Characteris- tics	Prevention of Crack, Quality Assurance of Scribe
	Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
	Chip Scribe		Appearance of Chip	
	Appearance OPQC Lot Judgement		Jan Character A vi mile	
Frame-	Martine C ans q			
near	Assembling	Assembling	Appearance after Chip Bonding Appearance after Wire Bonding	Quality Check of Chip Bonding Quality Check of Wire Bonding
	◇PQC Level Check		Pull Strength, Compression Width, Shear Strength	Prevention of Open and Short
	Inspection after Assembling		Appearance after Assembling	
D. al	◇PQC Lot Judgement		airs Engineering Deau	
rackage-	Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
	◇PQC Level Check	Marking	Marking Strength	
	 Final Electrical Inspection ◇Failure Analysis 		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Infor-
	Appearance Inspection			Action Constitution
	Sampling Inspection on Products	W 10 100		
	Receiving			
	Shipment			

3.3.3 Final Product Inspection and Reliability Assurance

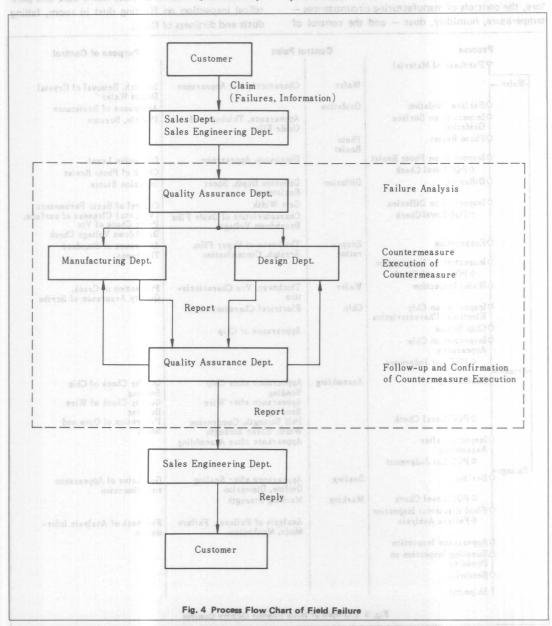
(1) Final Product Inspection to some all auditores as

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by

mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.



1. Inspection Method

Compared to conventional core memories, all peripheral circuits such as the decoder circuit, write circuit, read circuit, etc., are contained within the IC memories. As a result, all works of assembling the parts and performing electrical inspection, which had been carried out by core memory manufacturers in the past, have be come to be incorporated as works of IC manufacturers. Consequently, the electrical inspection of the memory IC has been faced to a more systematic inspection method and conventional IC inspection facilities have become completely useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a comparatively simple DC parameter facility. However, when the address input becomes multiplexed as in 16K memory, even the generation of the function test pattern becomes a serious problem. In the memory IC inspection, its quality cannot be judged by only inspecting DC characteristics related to external pins. This is because numbers of transistors, etc., related to the DC characteristics of the pins only amount to 1/1000 of all element numbers within IC memories. The following various address patterns are proposed to inspect whether or not the internal circuits are functioning correctly.

- (1) All "Low", all "High"
- (2) Checker flag has be your amount to sign as it is get
- (3) Stripe pattern
- (4) Marching
- (5) Galloping
- (6) Walking
- (7) Ping-pong

Although there are a lot of address patterns, only representative ones have been listed. These patterns are convenient for checking the mutual finterference of bits and sometimes are patterns with maximum power dissipation. Among the abovementioned patterns, those of (1) to (4) are the socalled N patterns and these patterns are capable of checking IC memories of N bits with several sequences of N at most against the memory IC of N bits. Whereas, those of (5) to (7) are called N² patterns and they need patterns several sequences of N².

A serious problem arises in using the N² patterns in a large-capacity memory, for example, a long period of about 30 minutes becomes necessary to perform inspection of the 16K memory with galloping pattern. Patterns from (1) (3) are comparatively simple and good methods, but they are not perfect against a failure in the decoder circuit. As the most simple pattern for inspecting the necessary memory function, there is a "Marching" pattern.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits written in "0"s. The addressing method will be explained for a simple 16 bit memory as an example.

- (1) Write "0" for all bits Fig. 1(a)
- (2) Read "0" of 0th address and check that the read data is "0". Hereafter, the meaning of "Read" is "checking and judging the data".
- (3) Write "1" in the 0th address Fig. I(b)
- (4) Read "0" of 1st address
- (5) Write "1" in 1st address
- (6) Read "0" of nth address
- (7) Write "1" in nth address Fig. 1(c)
- (8) Repeat above procedures (6) and (7) up to the last. Finally, all data will become "1".
- (9) Since all data are "1"s in this condition, replace "0" and "1" after procedure (2) and repeat once more up to procedure (8).

It is understood that 5N address patterns are necessary for the N bit memory in this method.

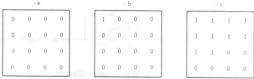


Fig. 1 Addressing method for 16 bits memory in the Marching pattern

3. Generation of Marching Pattern

The method of generating the marching pattern and displaying failed bits of the memory on the Braun tube will be introduced. Fig. 2 shows the all block diagram. The address pattern is generated by using four synchronous 4 bit counters. All address patterns are shown in Fig. 4. This example, is for 16K bit memory, however, it can be easily understood that A14 which has a half frequency of the maximum address input A13 is the same as the data input.

The A15 signal together with the carrier signal of HD74161 is used to determinine the termination of the sequence.

As shown in Fig 2. In the read and write cycles after cleaning all bits addressing is twice the period of clearing. This switching is performed at the gate of

the binary circuit following the reference pulse generating circuit.

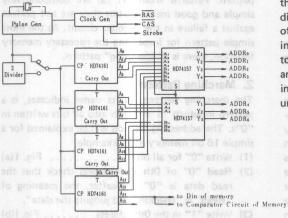


Fig. 2 Marching Pattern Generating Circuit

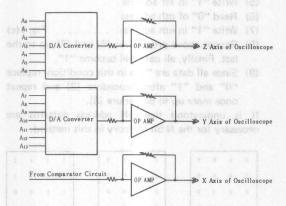


Fig. 3 Fail Bit Map Display Circuit

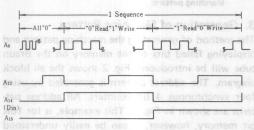
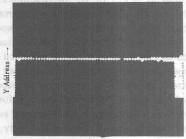


Fig. 4 Entire Pulse Relations

Input the output of HD74161 is input to the D/A converter and the output of D/A converter is connected to the oscilloscope to display \rightarrow X-Y matrix. The output of the comparator circuit is connected to the Z axis and performs luminous intensity modulation. In this way, the fail bit map can be displayed on the CRT. Fig. 5 shows an example checking a voltage margin. By changing the

power voltage V_{BB}, the increase and decrease of the failed bits can be well understood. The operation of the memory can be dynamically understood by displaying its operation on the CRT. The operation of the memory IC is extremely complicated differing from other TTLs, etc.. Its operation is not easy to understand by pulse waveform observation with an ordinary oscilloscope. The fail bit map as shown in Fig. 5 is extremely useful. It is capable of visually understanding the operation of memory IC.



(a) VBB -0.3V X Address --

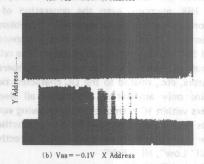


Fig. 5 Example of Dependency of Fail Bit Map on VBB

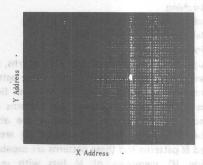


Fig. 6 Example of 1 bit solid fail

4. Failure Mode and the bear year that accepts to

Generally, failure $70\% \sim 90\%$ of failures at users are of those called solid failure. This failure mode has no relation with access time, voltage margin and timing, and is not capable of reading from or writing to certain specified bits and is failure fixed to "0"

or "1". An example of single bit solid failure is shown in Fig. 6. The convenient checker, previously mentioned as simple tester, is sufficiently capable of detecting such failures. Therefore, with the exception of special cases, it can be considered that the necessity of performing high-precision measurements such as those made by memory IC manufacturers is rare.

In the inspection of memory IC at our company, full inspection under the worst conditions are performed so as to guarantee sufficient operations under all power voltage conditions and timing conditions listed in the data sheet.

An extremely accurate memory tester becomes necessary for performing high-precision inspection with 1ns accuracy. Our company is developing IC memory testers to supply memory ICs with excellent characteristics and quality to users and is establishing the system capable of developing further high-efficiency memory ICs.

APPLICATION OF DYNAMIC RAMS

1. Power On

After turning on power to set the memory circuitry, hold for more than $500\mu s$ and apply eight or more dummy loads before actuating the memory. The dynamic cycle may be either an ordinary memory cycle or a refresh cycle. When power is turned on, power-on current flows which varies with the rise time of V_{CC} and clock conditions, as shown in Fig. 1. If the rise time is $10\mu s$ or thereabout, the RAM does not operate dynamically and through-current passes to the internal inverter since the potential at the internal circuitry becomes unstable. Nevertheless, this through-current decreases as the operation of the internal circuitry becomes stable. With all this in mind, rise time of not shorter than $100\mu s$ is recommended for power-up.

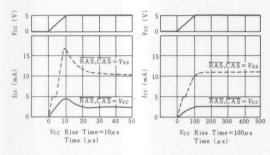


Fig. 1 Relationship between standard value of Icc and Vcc during power-up

2. Operation Modes (See Fig. 2)

(1) Read Cycle:

First, decide the X address of the memory cell chosen and start with trailing of \overline{RAS} . When the X address has been held by the internal circuitry, change it to Y address. Then, trail \overline{CAS} to take in the Y address. If the \overline{WE} pin is at high level, output will appear on the Dout pin after a certain time.

(2) Write Cycle:

The input at Din is written in the memory cell when \overline{WE} turns to low level before \overline{CAS} .

(3) Read/Modify/Write Cycle:

During this cycle, \overline{CAS} and, then, \overline{WE} are trailed down to low level so that data is read out from and written in the same address with in the same memory cycle.

(4) Page Mode Cycle:

In this cycle; \overline{CAS} is cyclically moved, after taking in the X address through \overline{RAS} , to scan only the Y address. This permits reading out and writing in only one column data at high speed.

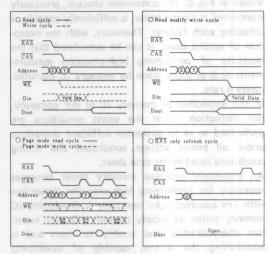


Fig. 2 Operating modes of Dynamic RAMs

2. Data Output

Dout is a TTL-compatible three-state output with two \overline{TTL} -load fan outs. The output is controlled by the \overline{CAS} signals; it is held while \overline{CAS} is low, while Dout returns to a floating state when \overline{CAS} is high. In the early write cycle, the output becomes a high-impedance one to permit the use as a common I/O terminal.

3. Refreshing

Refreshing is a process of periodical rewriting to make up for the leakage of the charge accumulated in the memory cell. This operation is implemented in the RAS only refresh cycle, ordinary read cycle, and so on. Whether 16k- or 64k-bit, all bits can be refreshed by giving a 128-cycle scanning to only the X addresses between A0 and A6. To be more specific, each cycle refreshes 128 bits for the 16kbit Dynamic RAMs and 512 bits for the 64k-bit RAMs. Especially, the RAS only refresh cycle permits such a power-efficient refresh as calls for only approximately 75 percent of the current consumed by the read cycle. With CAS fixed at high level, the output is a high-impedance one. The HM4816A has a special function called the hidden refresh which enables holding the output by turning CAS to "low" while RAS only refresh is on. There are two methods of refreshing: concentrated and deconcentrated refreshing. The former gives a concentrated 128-cycle refresh after operating the memory for a period of 2ms maximum. In contrast, the latter repeats a refreshing cycle every 16µs following the initial 16µs (=2ms/128) memory operation. A choice between the two modes calls for a careful consideration about the system's efficiency.

4. Operating Current for Dynamic RAMs

Fig. 3 shows the waveforms of the current applied in various operating modes (HM4864). The mean operating current in each mode equals the value obtained by dividing the integrated result of each waveform by the cycle time. The first peak current in each operating mode appears as a result of the circuit operation during the memory access time. On the other hand, the peak current during standby appear as a result of the precharging operation in each circuit. Having two circuitry operation modes - X and Y. Dynamic RAMs show different peak currents depending upon the operating timing of RAS and CAS. That is, the greatest peak current appears when both X and Y circuits operate simultaneously. The maximum peak current for the HM4864, for example, is approximately 100mA. The current consumed while the memory stands by on the board is expressed in terms of the cycle time dependency shown in Fig. 4. During standby, with a once-in-every 16µs refresh, the HM4864 consumes approximately 3mA of current.

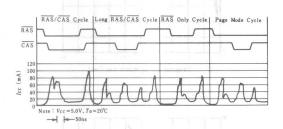


Fig. 3 Power supply voltage (HM4864)

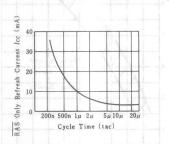


Fig. 4 Cycle time dependence of RAS only refresh current (HM4864)

5. Noise

Broadly, noise can be classified into power source noise and input signal noise. With the latter, furthermore, whether it is an overshoot or undershoot must be considered. The overshoot should be

held below the highest input level specified. As to the undershoot, the input-undershoot-induced parasitic transistor effect in the input area is prevented by providing a -5V VBB to the three-way power source and a built-in bias circuit on the substrate. Normally, design should be such that the input undershoot does not exceed the minimum value specified for VII, at worst. The power source noise can be further classed into low-frequency noise and high-frequency noise as shown in Fig. 5. To assure a stable memory operation, the peak-to-peak power supply voltage in the presence of low- or highfrequency noise should be held below 10 percent of its standard level. Overshoot and undershoot can be reduced by inserting a damping resistance of several tens of ohms in Dynamic RAM series. To prevent the power source noise, it is recommended to provide a condenser of $0.1\mu F$ or so to each one or two devices.

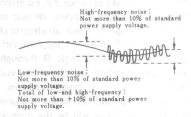


Fig. 5 Power source noise



PROGRAMMING & ERASING OF PROMS

1. PROGRAMMING & ERASING OF EPROM

1.1 Programming to a Vd- s priblyong yet be

Information is programmed into the memory cell of an EPROM by applying a high voltage to its drain and gate (Fig. 1 and 2). The high voltage at the drain increases the energy of the electrons in the channel area. When the energy becomes high enough, the electrons become what are known as "hot electrons" that are capable of jumping across the oxide film. Pulled by the high voltage at the gate, the hot electrons are admitted into the floating gate. The electric charge entering the floating gate changes the threshold voltage in the memory element, whereby it is stored as new information. When reading out, voltage is applied as shown in Fig. 3, and "1" and "0" are identified by checking whether or not current flows. Since the drain voltage for read-out is set at about 3V, no erroneous writing takes place. When shipped, all bits of the EPROM are held at logic "1" with all electric charge released (with no information programmed in). By changing the logic 1 to logic 0 through the application of the specified waveform and voltage. the necessary information is programmed in. The higher the Vpp voltage and the longer the program pulse width tow, the more will be the quantity of electrons to be programmed in, as shown in Fig. 4. If the VPP exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check Vpp overshoot by the PROM programmer and take all other possible caution. Also with for the negative-voltage-induced noise at other terminals, since it can touch off a parasitic transistor effect and apparently reduce the yield voltage Hitachi's EPROMs are usually capable of being written and erased more than 100 times, although the number of times is not guaranteed because it is difficult to give an exhaustive inspection prior to shipment. At any rate, 100 times is enough since the frequency of reprogramming in practical application rarely exceeds about 10 times.



Fig. 1 Memory transistor circuit symbols

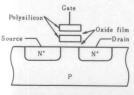


Fig. 2 Cross section of memory transistor

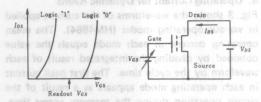
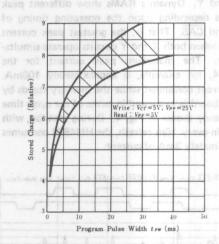


Fig. 3 Reading out stored information



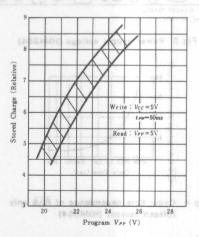


Fig. 4 Typical Programming Characteristics of EPROMs.

1.2 Erasing

Data strored in the EPROM is erased by releasing the electric charge from the floating gate through the exposure of the memory chip to ultraviolet light. Light has an energy that is inversely proportional to its wavelength. Receiving the energy of the ultraviolet light, the electrons in the floating gate are again turned into hot electrons, which jump across the oxide film into the control gate or substrate. As a result of this process, the stored information is erased. Accordingly, the stored information can not be erased by such lights whose wavelengths are too long to give adequate energy to jump over the barrier of the oxide film, For successful erasing, the wavelength and minimum exposure rate of ultraviolet light are specified as 2,537Å and 15W sec/cm² respectively. This condition is attained by exposing a device to an ultraviolet lamp of $12,000\mu\text{W/cm}^2$ $1.2 \sim 3\text{cm}$ away for approximately 20 minutes. The ultraviolet light transmission rate of the transparent lid is about 70 percent. Any contamination or foreign material at the surface of the capsule lowers the transmission rate, prolonging the erasing time. So such contamination should be recovered by use of alcohol or other solvent that does not damage the package. Fig. 5 shows typical erasure characteristics for EPROM.

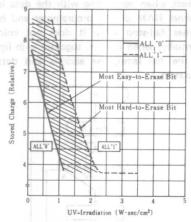


Fig. 5 Typical Erasing Characteristics

1.3 Data retention characteristic of EPROM

As a result of writing in, approximately 0.5 to 2.0 x 10⁻¹³ coulomb of electrons are accumulated at the floating gate. With the elapse of time, however, these electrons decrease, as a result of which the inversion of stored information can happen. The mechanism of electron dissipation is generally explained as follow:

(1) Data dissipation by heat

The accumulation of electrons at the floating gate is an unbalanced state, so the dissipation of thermally excited electron is unavoidable. Therefore, the data holding time has a close relationship with temperature. Fig. 6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

(2) Data dissipation by ultraviolet light

Ultraviolet rays at a wavelength of not greater than 3,000 ~ 4,000Å is capable of releasing the electric charge stored in the memory of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet rays. so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Fig. 7 shows examples of the data retention time under an ultraviolet eraser. sunlight and fluorescent lighting. But it should be noted that the data for fluorescent light and sunlight are not definite because of their varying ultraviolet ray contents. The ultraviolet ray content in sunlight, for example, varies greatly with seasons, weather and the composition of the atmosphere.

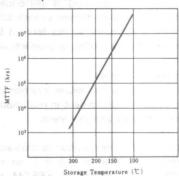
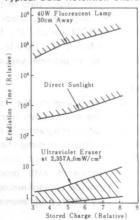


Fig. 6 Typical Data Retention Characteristics



(3) Data dissipation by voltage

This type of data dissipation occurs while information is being written in. At other memory cells lying on the same word line or data line as the memory cell being programmed, high voltage can cause the dissipation of stored electric charge. Of course, such defects are removed at the factory by pre-shipment inspection. The programming voltage and pulse width should be always kept within the specified range for the same reason.

1.4 EPROM Programmer

The 16K EPROM Programmer stores the program in its internal RAM and writes the program in the EPROM. For this programming, the minimum of 3 functions, the Blank check function prior to programming, the programming function and the Verify function after programming are necessary. As shown in the drawing, there are also programmers provided with a reverse insertion checking function or pin contact checking function prior to the Blank Check. The outline of each block is as follows.

(a) Pin contact check

In the connection test of the ROM pin and the socket, normally checking is performed by detecting the forward current of each EPROM pin. Care is necessary as this forward biased resistance differs according to products of each company.

(b) Reverse insertion check

This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.

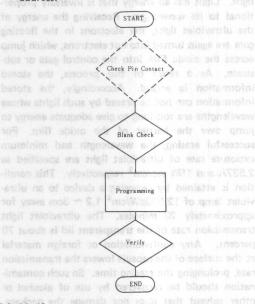
(c) Blank check

This check is performed prior to programming and checks whether or not it is an erased EPROM or for preventing EPROM reprogramming. Since the output data in the erased condition are "1" (high level), check whether or not data in EPROM are all "1". It willfailstop even when 1 bit of "0" (low level). Normally, it is designed to provide warning with a lamp or buzzer.

(d) Programming

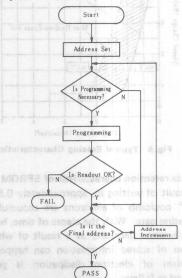
The function of programming the data in the internal RAM of the programmer into EPROM and will fail-stop when programming cannot be made. The normal flow is as shown below. The EPROM data will be read out prior to programming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be

performed. Then, read out will be made again and compared with the programming data, and if they coincide, it will progress to the next address.



(e) Verify

This function is for checking after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer and it performes fail-stop when it does not coincide. Normally, when it fails, together with lighting of the fail lamp, the address and data are displayed.



(f) How to input the program

There are the following methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and retypewriter input are options.

Method	Content					
Copy input	Input by copying the master ROM.					
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program					
Paper tape input	Read the paper tape furnished from the host system with the tape reader					
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.					

1.5 Handling EPROM

When brought in contact with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write marging setting that give a wrong impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges through the eradiation of ultraviolet rays for a short time. It is recommended to execute reprogramming after this eradiation since it reduces the electric charges in the floating gate, too. The basic cluntermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

- Establish a ground for the operator to handle EPROM. Avoid the use of gloves etc. that may develop a static charge.
- (2) Refrain from rubbing the glass window with plastics and other substances that may develop a charge.
- (3) Avoid the use of coolant sprays which contain some ions.
- (4) Use shielding labels (especially those containing conductive substances) that can evenly distribute the established charge.

1.6 Shielding label

When using an EPROM in an environment where ultraviolet exposure can occur, it is advisable to put a shielding label on its glass window to absorb ultraviolet light. Specially prepared shielding labels are

marketed. Metal-loaded labels are particularly effective. In choosing a shielding label, the following points should be carefully checked.

(1) Adhesiveness (mechanical strength)

Avoid repeated attaching and dusting that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on the old one since peeling may develop a static charge.)

(2) Allowable temperature range

Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may come off easily. When it sticks too fast, the paste may remain on the window glass even after the label has been removed.

(3) Damp-proofness

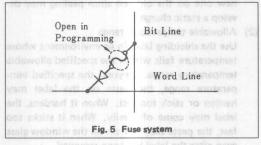
Use the shielding label in an environment whose humidity falls within the specified allowable humidity range. Today there are few shielding labels that can meet all environmental requirements established for the EPROM. So a suitable one must be chosen for each specific application.

2. PROGRAMMING OF BIPOLAR PROMS

2.1 Programming System

The storing system of the Bipolar PROM can be generally classified into 2 systems; the Blown diode system and fuse system.

The latter is a system in which the metal-made fuse is burned off by current (Fig. 5). In the former, Emitter-Base junction is short-circuited by AI, which has penetrated into Base because of current



2.2 Programming Method

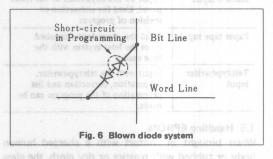
Programming is executed by the conventional programming equipment (PROM writer) using a board suited to the product.

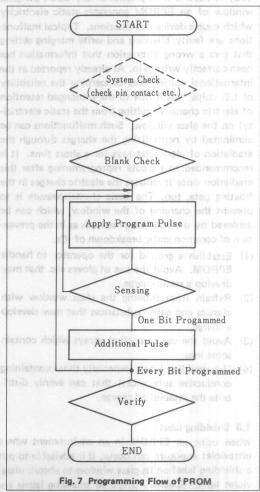
First, check if all bits are programmable (Blank check), next write the pattern you want to program one by one bit. At every application of current pulse, confirm that program is available by sensing output level. And when programming has been completed, apply additional pulse. This process should be performed for all bits into which you want to write, and as you have completed programming, check (Verify) if you have programmed in the same pattern as you intended. If you do not find any mistake, programming has been completed.

For Blank check, Sense and Verify whether output pin level is high (non-programmed) or low (programmed) is checked by sense current (Is). Vs — Is characteristic of normal series and S series is shown in Fig. 8 and 9, respectively. Specified value of sense current (Is) of both normal series and S series is 20 mA, and voltage reference level is 7.5 V.

Fig. 10 and 11 show the relation between program current and program pulse number necessary for 1 bit to be written. With consideration of its influence on breakdown voltage, program current is specified as 130 mA in normal series and as 90 mA in S series.

pulse applied to E-B junction (Fig. 6). Generally, the blown diode type is considered to be more reliable. A grow back phenomenon, that is, migration and recombination of the metal, is seen in fuse system. HITACHI devices use the blowin diode system.





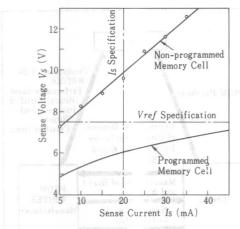


Fig. 8 Vs - Is Characteristic of Normal Series (HN25089)

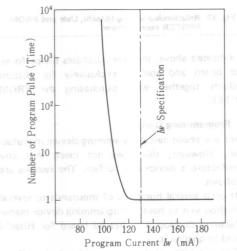


Fig. 10 Program Pulse — Iw Characteristic of Normal Series (HN25089)

2.3 Programming Characteristics of Hitachi Bipolar PROM

Small program current

130 mA for normal series, and 90 mA for S series are required for programming. Therefore, there are few bad effects caused by breakdown voltage degradation and parasitic effects.

Fast programming speed

As seen in Fig. 10 and 11, program pulse for 1 bit memory cell can be mostly written at one time Consequently, the program time per device is quite short. In case of 8K bit, for example, only 2 or 3 seconds at an average are required.

High programming yield

Unlike the MOS PROM, the Bipolar PROM cannot be rewritten, once it is written into the memory

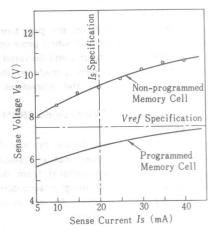


Fig. 9 Vs - Is Characteristic of S Series (HN25169S)

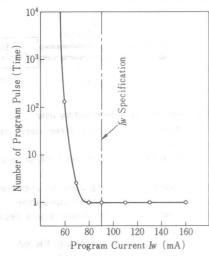


Fig. 11 Program Pulse — Iw Characteristic of S Series (HN25169S)

cell.

Therefore, it does not allow programming and inspection of the product prior to delivery. Due to this, sometimes a defective product (which does not allow programming) might be delivered.

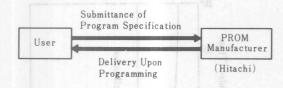
Generally, the programming efficiency percentage is 90~95% when programming is performed on the user's side. Special tests such as actually performing programming on the dummy cell in the chip, performing continuity test of all memory cells, etc., are made prior to delivery for minimizing the possiblity to deliver defective products.

2.4 Programming

There are two methods in the programming of PROM. That is, the method when programming is made by PROM manufacturer and delivered and the method when programming is made on the user's side. Both these methods and procedures will be explained below.

2.4.1 Programming performed by the PROM manufacturer

As shown in the drawing below, the manufacturer receives the program specification (specification designating the program pattern) from the user, performs writing (Programming) in accordance with the specification and performs delivery. In this case, a special writing fee is charged.

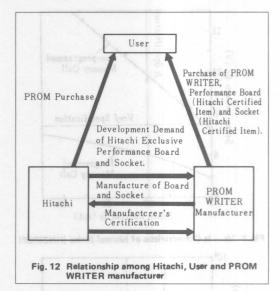


2.4.2 Programming performed by user

In this case, the following three items must be prepared by the user.

- 1 PROM WRITER (Main unit of programming equipment)
 - One capable of being used in common with equivalent products of other companies.
- 2 Performance board (Exclusive board designated by each manufacturer)
 - Minimum of 1 board for Hitachi PROM.
- 3 Sockets (sockets suited to product) Minimum of one socket per product. These sockets are purchased from the PROM WRITER manufacturer.

The relationship among PROM WRITER manufacturer, Hitachi and user is shown in Fig. 12.



As indicated above, the user purchases the performance board and sockets exclusively for Hitachi products together with purchasing the PROM WRITER.

2.5 Programming Device

There are about ten programming device manufacturers. However, this does not mean that any manufacturer's device will suffice. The reasons are as follows.

- It costs several hundreds of thousands or several million yen to have a programming device manufacturer develop a dedicated board for Hitachi and to qualify it.
- The suitability of the programming device affects the programming efficiency. Therefore, it should be a device of a reliable manufacturer.
- The servicing setup for handling troubles should be consolidated. The setup should be one that judgement can be accurately made on whether it is a writing device trouble or PROM trouble.

Hitachi has prepared a list of recommended manufacturers which meet the above requirements. Please contact our sales engineering staff for information in this regard.

■ MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into the mask ROM is performed by the CAD system using a large-sized computer. You should submit the data of the ROM code in conformity with the specification explained below by either paper tape, EPROM or magnetic tape. In addition, enter your instructions such as the chip select, customer part number, etc., in the "ROM Specification Identification Sheet" and attach it to the ROM code data.

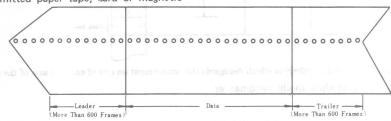
1. Overall Specification

Since the submitted paper tape, card or magnetic

tape is fed into the large-size computer as it is, observe the following specifications.

1.1 Specification of Paper Tape

- 1.1.1 Any color paper tape may be used as long as it is a marketed 1 inch wide paper tape for computers. However, a black color paper tape is recommended.
- 1.1.2 Take more than 600 frames for the leader and trailer.



1.1.3 Parity mode

The presence and type of parity are clearly described in the "ROM Specification Identification Sheet".

There are following modes in the parity system.

(1) With parity

Even parity EVEN Odd parity ODD

- (2) Without parity
- 1.1.4 Use the 8 unit ASC11 code as the code.

1.2 Specification of Magnetic Tape

- 1.2.1 Use the following type of magnetic tape which can be netered in a magnetic tape device which is compatible with the IBM magnetic tape device.
- (1) Length 2,400 feet, 1,200 feet or 600 ffet

- (4) Bit density 800 BPI or 1,600BPI (Clearly state which it is in the "ROM Specification Indentification Sheet".)
- 1.2.2 Use the EBCDIC code as the use code.
- 1.2.3 Make the format of the magnetic tape as described below.
- (1) No leading tape mark
- (2) No label

- (3) Record size 80 byte/1 record
- (4) Block size 10 records/1 block
- (5) The end of the file should be indicated by 2 successive tape marks (TM).
- 1.2.4 Ensure that the magnetic tape becomes of 1 roll for each chip. Since extending the single-chip portion over several rools is impermissible, submit by compiling into the single-chip portion for each roll.

2. Data Mode

2.1 HMCS6800 Load Module Mode

This mode is the object mode output from the assembler of HMCS6800.

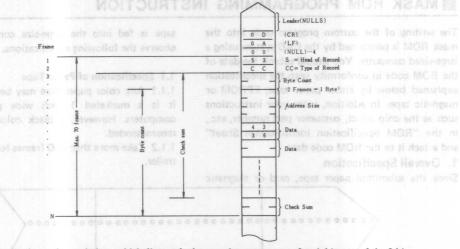
2.1.1 Divide the 8 bit code into the upper and lower 4 bit codes and convert each into hexadecimal notation.

(Example) The code of 1100 0110 becomes as follows under binary notation.

(Upper 4 bits	(Lower 4 bits)	Bit weight
D, D, D, D,	$D_3 D_2 D_1 D_0$	(ROM output
1 1 0 0	0 1 1 0	equivalence)

2.1.2 The composition of the load module mode is shown below by taking the case of paper tape as the example. The numbers written in the tape are ASCII code hexadecimal numbers of the data.

B O T	Block 1	Block 2	Block 3		T M	T M	E O T
-------------	---------	---------	---------	--	--------	--------	-------------



(Note) The check sum is a technique which disregards the complement on one of each bit sum of the 8 bits.

2.1.3 The actual load module mode becomes as shown below.

		CC=30	CC=31	CC=39	
Frame		Header record	Data record	End of file record	
1 //	Record Start	5 3 S	5 3 S	5 3 S	
2	Record Type	3 0 0	3 1 1	3 9 9	
3	Byte Count	3 0 0 6	3 1 1 6	3 0 0 3	
5 6 7 8	Address Size	3 0 3 0 0000 3 0 3 0	3 1 3 1 3 0 3 0	3 0 3 0 3 0 3 0	
9 10	Data	3 4 3 8 48-H	3 9 3 8 9 8	4 6 4 3 FC (Check Sum)	Without parity 1.4 Use the 8 u
sboM's	Data	3 4 3 4 44-D	3 0 3 2 0 2		
	Data o sril	3 5 3 2 52-R			
orni e	Check Sum	3 1 4 2 1B (Check Sum)	4 1 3 8 A8 (Check Sum)		

S0 indicates the head of the file and S9 indicates the end of the file. The actual data enters following S1. It means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by

counting in increments of 1 byte of the data and checking whether it is sequential or not. In places where the address is skipped, the data of 00 or FF enters hexadecimally. The printed example of the paper tape of the HMCS6800 load module mode is as shown below.

Example Header Record →S00B000058204558414D504CB5 Data Record →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24 Data Record →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06 End of File Record →S9030000FC

- 2.1.4 The ROM code data are capable of handling the following 4 types of cases. A header recorder is required in front of the data recorder and an end of file recorder at the back of the data recorder.
- Case when the data reaches full capacity of ROM

The ROM recorder for 1 chip enters into the data recorder. Since the address of the address size of the



data recorder counts the data and checks whether or not it is in a sequential address, it becomes necessary that the address not be skipped. The ROM head address column of the "ROM Specification Identification Sheet" becomes 0.

(2) Case when data is input from en route of ROM



In this case, perform entry by decimal notation in the ROM head address column of the "ROM Specification Identification Sheet" on which ROM address you wish to input the data. The data 00 or FF will enter into the blank address by hexadecimal notation.

(3) Case when data is input by skipping intermediate address



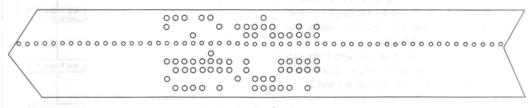
The address of the address size of the data recorder is counted in increments of 1 byte of the data, compared with the next address of the data recorder and checked whether or not it is sequential. The data 00 automatically enters by hexadecimal notation into the ROM code of the skipped address. Therefore, the writing of data as in the following drawing is also possible. In this case, perform entry into the "ROM Specification Identification Sheet" that the ROM head address enters from 0 address for data I and from which address it enters for data

(4) Case when the data is less than the full capacity of ROM



In case the data volume is less than the total byte capacity of ROM LSI when the end of file recorder appears, it becomes written as the ROM code as shown in the following drawing.

(Example) Indicates the example of the paper tape when the data recorder is S1141920B6-FC ...



2.2 BNPF Mode

2.2.1 One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F. 2.2.2 The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.

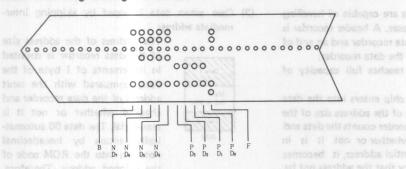
(Example) The code of 0F by hexadecimal notation is symbolized as shown below (in case of paper tape)

2.2.3 It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specifica-

tion Identification Sheet" always becomes 0.

В								,	Indicates start of 1 word.
N								,	Indicates "0" of 1 bit data.
Р									Indicates "1" of 1 bit data.
F					٠				Indicates end or 1 word.





Note 1) Sometimes X is used besides P and N in the display of the word content by the BNPF slice.

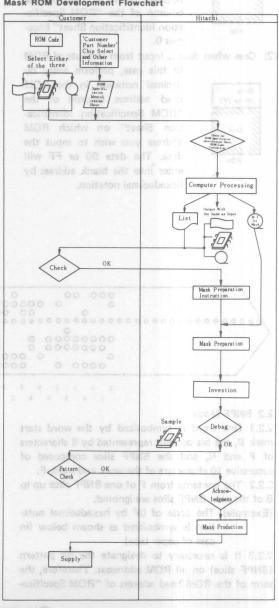
> X means that the user is not concerned whether the bit is P or N. However, since it is necessary to decide the P or N for performing tests, Hitachi performs selection of P or N. The results are informed by making entry in the identification table.

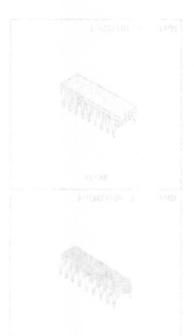
Note 2) The contents of the BNPF slice are not only those with the continuation of PN and the form of B*nF can also be used. This means that the content of the slice existing just prior to this word will be repeated for n words from this word.

For example, when B*4F exists at the 10th word, it means that the content of the 9th word will be repeated in the 10th, 11th, 12th and 13th words. (However, it does not necessarily follow that the X content of Note 1 above will be repeated.) n shall start from 1 and be a number below the total addresses of ROM.

Note 3) When a certain block is not used (when an unused ROM address exists), disposition can be made by utilizing Notes 1 and 2.

Mask ROM Development Flowchart





DATA SHEETS

MOS STATIC RAM



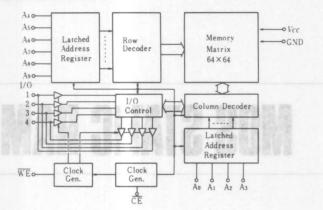
HM4334-3, HM4334-4 HM4334P-3, HM4334P-4

1024-word×4-bit Static CMOS RAM

FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation;
- Standby: Operation:
- 10μW (typ.) 20mW (typ.)
- Access Time; HM4334/P-3:
- 300 ns (max.) 450 ns (max.)
 -) (5V±5%)) (5V±10%)
- HM4334/P-4:
- Directly TTL Compatible: All inputs and outputs
 Common Data Input and Output using Three-state Outputs
- On Chip Address Register

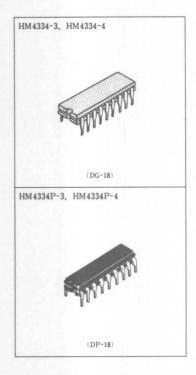
BLOCK DIAGRAM



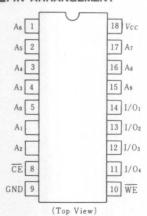
MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin*	V_T	-0.3 to Vcc +0.5	V
Power Supply Voltage*	Vcc	-0.3 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	Tate	-55 to +125	°C
Storage Temperature (Cerdip)	T_{stg}	-65 to +150	°C

^{*} with respect to GND



PIN ARRANGEMENT



■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

τ.	C		HM 4334/P-	The state of the s		HM 4334/P -4			
Item	Symbol	min	typ	max	min	typ	max	Unit	
Supply Voltage	Vcc	4.75	J05.0 VO	5.25	4.5	5.0	5.5	V	
	GND	0	0	0	0	0	0	V	
	V_{IH}	2.4	_	Vcc+0.5	2.4	_	Vcc+0.5	V	
Input Voltage	V_{IL}	-0.3	YYYY	0.8	-0.3	X	0.8	V	

■DC AND OPERATING CHARACTERISTICS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, \text{ GND}=0\text{V}, \text{ HM4334/P-3}: V_{cc}=5\text{V}\pm5\%, \text{ HM4334/P-4}: V_{cc}=5\text{V}\pm10\%)$

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}	-1.0	_	+1.0	μΑ
Output Leakage Current	ILO	$\overline{CE} = V_{IH}$, $V_{out} = 0$ to V_{CC}	-1.0	_	+1.0	μΑ
0 B C	Icci	$\overline{CE} = 0V$, $V_{IN} = V_{CC}$, $I_{I \neq 0} = 0$	_	_	1.0	mA
Operating Power Supply Current	Iccz	$\overline{\text{CE}} = 0.8 \text{V}, \ V_{IN} = 2.4 \text{V}, \ I_{I \times O} = 0$	\ () -	2.5	5.0	mA
Average Operating Current	Iccs	$V_{IN}=0$ or V_{CC} , $f=1$ MHz, duty 50%, $I_{I/O}=0$	-	4	7	mA
Standby Power Supply Current	IccL	$\overline{\text{CE}} \ge V_{cc} - 0.2 \text{V}$	_	2	100	μΑ
0	Vol	$I_{oL} = 2.0 \text{mA}$		-	0.4	V
Output Voltage	V_{OH}	$I_{OH} = -1.0 \text{mA}$	2.4	_	_	V

■CAPACITANCE $(Ta=25^{\circ}\text{C}, f=1\text{MHz})^{1}$ box 100 library in one as a second sec

Item	Symbol	Test Condition	min	typ	max	Unit
I/O Terminal Capacitance	C1/0	$V_{l \sim 0} = 0 \text{ V}$	1)(+)	7	10	pF
Input Capacitance	Cin	V _{in} =0V	_	3	5	pF

MAC CHARACTERISTICS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, \text{ GND}=0\text{V}, \text{ HM4334/P-3} : V_{cc}=5\text{V}\pm5\%, \text{ HM4334/P-4} : V_{cc}=5\text{V}\pm10\%)$

Te	C	1.1	ŀ	IM 4334/P -	-3	H	Unit		
Item	Syr	mbol	min	typ	max	min	typ	max	Unit
Read or Write Cycle Time*	TELEL	tc	460	_	- y	640	-		ns
Chip.Enable Access Time	TELQV	tAC			300		_	450	ns
Chip Enable to Output Active	TELQX	tcx	50	_	_	50	-	-	ns
Output 3-state from Deselection	TEHQZ	toffi	1723 -		100	_	_	100	ns
Write Enable Output Disable Time	TWLQZ	toff2	alls / =	7	100		_	100	ns
Chip Enable Pulse Width**	TELEH	tcE	300	-	_	450	_	_	ns
Chip Enable Precharge Time	TEHEL	tp and m	120	1200 m	7 1 miles	150	-	_	ns
Address Hold Time	TELAX	t _{AH}	100	_	_ 33.	100	_	_	ns
Address Setup Time	TAVEL	tas	20	V=101	JAV-3.	20	_	-	ns
Read Setup Time	TWHEL	trs	0	-	-	0	_	_	ns
Read Hold Time	TEHWL	t _{RH}	0	_	-	0	1—	_	ns
Write Enable Setup Time	TWLEL	tws	-20			-20	-	_	ns
WE to CE Precharge Lead Time	TWLEH	twpL	300	_	/-	450	_	_	ns
Chip Enable to Write Enable Delay Time	TELWL	tcwp	300	and Tart		450	_	_	ns
Write Enable Hold Time	TEHWH	t _{EWH}	0	-	_	0	_	_	ns
Write Hold Time	TELWH	t _{wH}	300			450	_	_	ns
Data Input Setup Time	TDVWH TDVEH	tos	200	Lad <u>18</u> 40		350	_	_	ns
Data Hold Time	TWHDX TEHDX	t _{DH}	0	-	Ē	0	_	_	ns
Write Data Delay Time	TWLDV	twos	100	23/_	_	100	_	_	ns
Chip Enable Rise/Fall Time	TT	t _T	_	-	300	_	_	300	ns

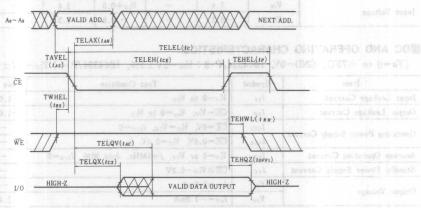
^{*} TELEL (t_c) = TELEH (t_{cE}) + TEHEL (t_P) + t_r (20ns) + t_f (20ns)

^{**} For Read Modify Write Cycle, TELEH(tcr) = TELWL(tcwo) + TWLEH(twpL) + t_f(20ns)



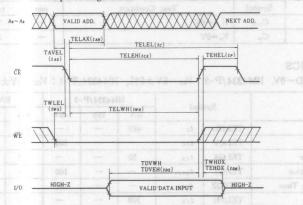
MAC TEST CONDITIONS

• READ CYCLE



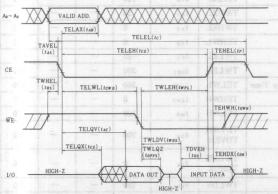
Note) *; TEHQZ (t_{OFF1}) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

• WRITE CYCLE



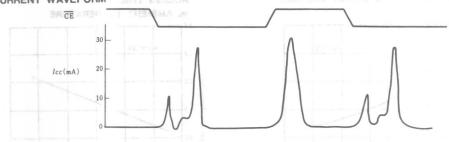
Note) t_{DS} and t_{DH} are measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.

• READ MODIFY WRITE CYCLE



*; TWLQZ (t_{OFF2}) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

● CURRENT WAVEFORM



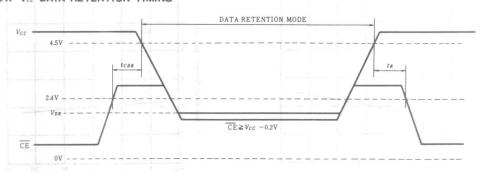
[NOTE] $V_{CC} = 5.0 \text{V}, T_a = 25^{\circ} \text{C}$

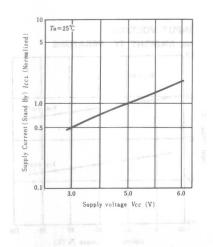
■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CE}} \ge V_{cc} - 0.2\text{V}$	2.0	_	_	V
Data Retention Power Supply Current	I_{CCDR}	$V_{DR} = 3.0 \text{V}$	_	0.5	50	μΑ
Chip Deselection to Data Retention Time	t_{CDR}		0	_	_	ns
Operation Recovery Time	t_R		t _{RC} *	_	-	ns

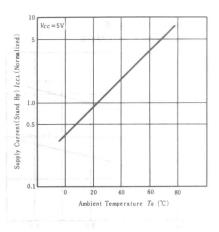
^{*} tRC=Read Cycle Time HOUD HOUS BOARDY

● LOW Vcc DATA RETENTION TIMING

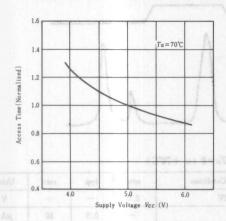




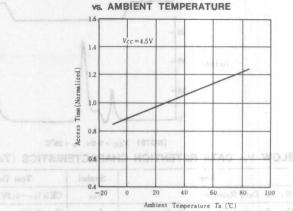
SUPPLY CURRENT VS. SUPPLY VOLTAGE SUPPLY CURRENT VS. AMBIENT TEMPERATURE



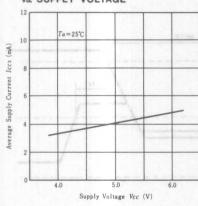
ACCESS TIME VS. SUPPLY VOLTAGE



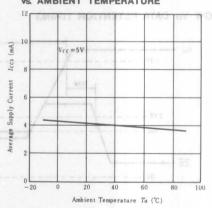
ACCESS TIME MROTEVAW THEREUS



AVERAGE SUPPLY CURRENT VS. SUPPLY VOLTAGE

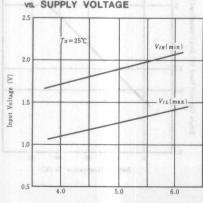


AVERAGE SUPPLY CURRENT WAS AMBIENT TEMPERATURE



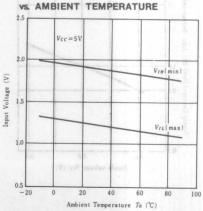
INPUT VOLTAGE VS. SUPPLY VOLTAGE

SUPPLY CURRENT . AMBIENT TEMPERATURE



Supply Voltage Vcc (V)

INPUT VOLTAGE



HM4334P-3L, HM4334P-4L

1024-word×4-bit Static CMOS RAM

FEATURES

- Single 5V Supply
- Low Power Standby and
 Low Power Operation;

Standby: 10 Operation: 20

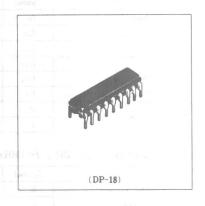
10μW (typ.) 20mW (typ.)

• Fast Access Time; HM4334P-3L:

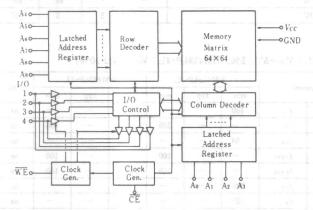
HM4334P-3L: 300 ns (max.) HM4334P-4L: 450 ns (max.)

) (5V±5%)) (5V±10%)

- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register



BLOCK DIAGRAM

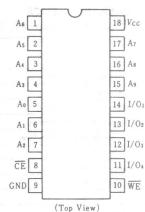


MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin*	V_T	-0.3 to Vcc+0.5	V
Power Supply Voltage*	Vcc	-0.3 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tets	-55 to +125	°C

^{*} with respect to GND

PIN ARRANGEMENT



PRECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	-	HM4334P-	BL sol	HM4334P-4L			
Item		min	typ	max	min	typ	max	Unit
S (0) V 100E	Vcc	4.75	5.0	5.25	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	0	0	0	V
T . 17 1.	V_{IH}	2.4	124621	Vcc+0.5	2.4	141313	Vcc+0.5	V
Input Voltage	V_{IL}	-0.3	_	0.8	-0.3	_	0.8	V

IDC AND OPERATING CHARACTERISTICS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, \text{ GND}=0\text{V}, \text{ HM4334P-3L} : V_{cc}=5\text{V}\pm5\%, \text{ HM4334P-4L} : V_{cc}=5\text{V}\pm10\%)$

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}	-1.0	_	+1.0	μА
Output Leakage Current	ILO	$\overline{CE} = V_{IH}$, $V_{out} = 0$ to V_{CC}	-1.0	vidau	+1.0	μΑ
0 .: P C 1 C	Icci	$CE=0V$, $V_{IN}=V_{CC}$, $I_{I \times O}=0$	best	thn a	1.0	mA
Operating Power Supply Current	Iccz	$CE=0.8V$, $V_{IN}=2.4V$, $I_{I\neq 0}=0$	100	2.5	5.0	mA
Average Operating Current	Iccs	$V_{IN}=0$ or V_{CC} , $f=1$ MHz, duty 50%, $I_{I>0}=0$	MH	141	182007	mA
Standby Power Supply Current	IccL	CE≥Vcc-0.2V (xapra) en 084 3.14-9408.	10014	2	20	μΑ
	Vol	IoL = 2.0mA stugged bas stugal IIA:	eldit=q	L-Com	0.4	V
Output Voltage	V_{OH}	IOH = -1.0mA DEC STATE SOUTH DETERMINED	2.4	pril <u>a</u> ts		V
			teralper	Essibi	DA GIAL	100

ECAPACITANCE ($Ta=25^{\circ}C$, f=1MHz)

Item	Symbol	Test Condition	min	typ	max	Unit
I/O Terminal Capacitance	C1/0	$V_{t \neq 0} = 0 \text{ V}$	-	7	10	pF
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	7 / -	3	5	pF

MAC CHARACTERISTICS

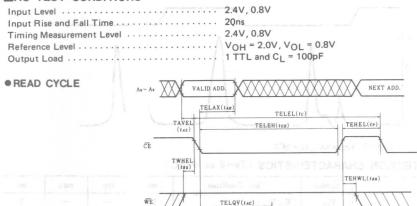
 $(Ta=0 \text{ to } +70^{\circ}\text{C}, \text{ GND}=0\text{V}, \text{ HM4334P-3L} : V_{cc}=5\text{V}\pm5\%, \text{ HM4334P-4L} : V_{cc}=5\text{V}\pm10\%)$

As 111 As				HM4334P-3L			HM4334P-4L		
Item	Syn	nbol	min	typ	max	min	typ	max	Unit
Read or Write Cycle Time*	TELEL	tc	460	Amoto.)		640			ns ns
Chip Enable Access Time	TELQV	tAC		100	300		_	450	ns
Chip Enable to Output Active	TELQX	tcx	50	Addres		50			ns
Output 3-state from Deselection	TEHQZ	toffi	-10	Regist	100	-	-	100	ns
Write Enable Output Disable Time	TWLQZ	toff2	-	-	100	Hook 1	_ + 89	100	ns
Chip Enable Pulse Width**	TELEH	tcE	300	i∂—sA		450			ns
Chip Enable Precharge Time	TEHEL	t _P	120	_	_	150	-	_	ns
Address Hold Time	TELAX	tah	100	-	-	100	_	-	ns
Address Setup Time	TAVEL	tas	20	-	SUM	20	MILLAN	3744	ns
Read Setup Time	TWHEL	trs	0	9 -	- Indiavé	0	T - 1	test -	ns
Read Hold Time	TEHWL	t _{RH}	0	0 E 0-		0	20.0		ns
Write Enable Setup Time	TWLEL	tws	-20			-20	Processing and the second	17 IF 100	ns
WE to CE Precharge Lead Time	TWLEH	twpL	300	-	-	450		_	ns
Chip Enable to Write Enable Delay Time	TELWL	tcwp	300			450		en codemic	ns
Write Enable Hold Time	TEHWH	t _{EWH}	0		-6.7	0	3/1019	radina r. A	ns
Write Hold Time	TELWH	twn	300	-	2013	450	_5/4	resource I	ns
Data Input Setup Time	TDVWH TDVEH	tos	200	awoo.	- SMITA	350	- 1971 (1971)	TO UT THE	ns
Data Hold Time	TWHDX TEHDX	t _{DH}	1888.0	-	ie ie	0	-	marl	ns
Write Data Delay Time	TWLDV	twos	100	_8/8	-	100			ns
Chip Enable Rise/Fall Time	TT	t _T	0.8_	20.1	300	1. Mar	-	300	ns

^{*} TELEL(t_c) = TELEH($t_{c\varepsilon}$) + TEHEL(t_P) + t_r (20ns) + t_f (20ns)

^{**} For Read Modify Write Cycle, TELEH(tce) - TELWL(tcwo) + TWLEH(twpL) + tf(20ns)

MAC TEST CONDITIONS



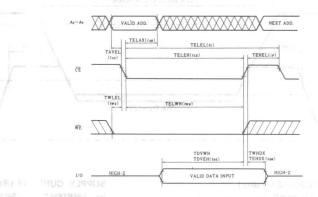
TELQX(tcx)

HIGH-Z

NOTE) *: T_{EHQZ} (t_{OFF1}) defines the time at which the outputs achieve the open circuit condition and is not referenced to outputs voltage level.

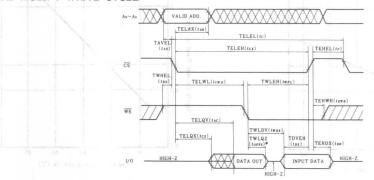
TEHQZ(toffi) *1

WRITE CYCLE



NOTE) t_{DS} and t_{DH} are measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.

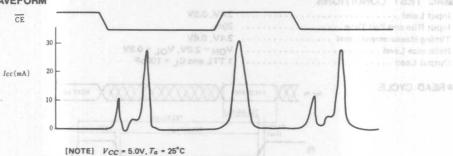
• READ MODIFY WRITE CYCLE



NOTE) *: TWLQZ (tOFF2) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.



CURRENT WAVEFORM

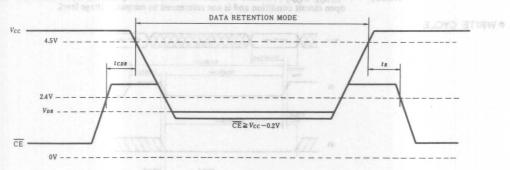


LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

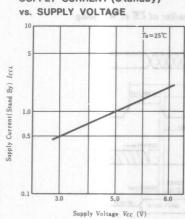
Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	<u>CE</u> ≥ <i>V_{cc}</i> - 0.2V	2.0	-	_	V
Data Retention Power Supply Current	ICCDR	$V_{DR}=3.0\mathrm{V}$	-	0.5	10	μΑ
Chip Deselection to Data Retention Time	tcor	THE EXTENSION OF	0	- I		ns
Operation Recovery Time	t _R		tRC*	-	_	ns

^{*} tac-Read Cycle Time

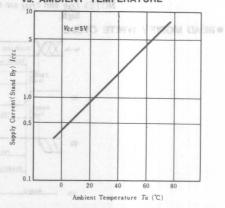
● LOW Vcc DATA RETENTION TIMING star to some out south of 19400 SOUTH (STOKE



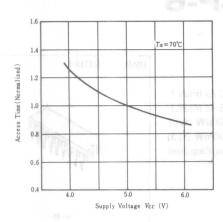
SUPPLY CURRENT (Standby)



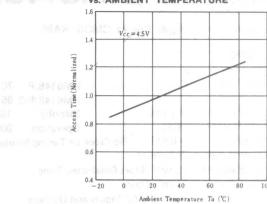
SUPPLY CURRENT (Standby) vs. AMBIENT TEMPERATURE



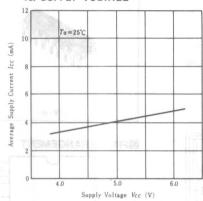
ACCESS TIME vs. SUPPLY VOLTAGE



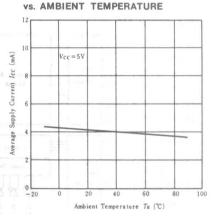
ACCESS TIME vs. AMBIENT TEMPERATURE



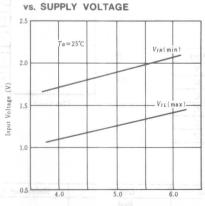
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



AVERAGE SUPPLY CURRENT

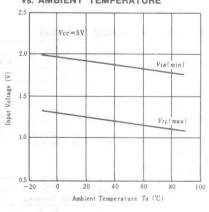


INPUT VOLTAGE vs. SUPPLY VOLTAGE



Supply Voltage Vcc (V)

INPUT VOLTAGE vs. AMBIENT TEMPERATURE



HM6148, HM6148-6 HM6148P, HM6148P-6

1024-word×4-bit High Speed CMOS RAM

FEATURES

- Single 5V Supply
- Fast Access Time

·HM6148/P 70 ns (max.)

HM6148/P-6 85 ns (max.)

 Low Power Standby and Low Power Operation;

Standby: Operation: 100μW (typ)

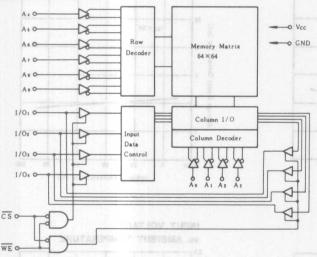
- Completely Static RAM;
- 200mW (typ) No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Pin-Out Compatible with Intel 2148

HM6148, HM6148-6 (DG-18)

HM6148P, HM6148P-6



BLOCK DIAGRAM



MABSOLUTE MAXIMUM RATINGS

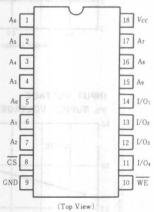
Item	Symbol	Value	Unit
Terminal Voltage*	V_T	-0.5△to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature (Plastic)	Tota	-55 to +125	°C
Storage Temperature (Cerdip)	Tata	-65 to +150	°C
Storage Temperature**	Tstg(biss)	-10 to +85	°C

^{*} with respect to GND. \triangle -1.0V (Pulse Width \leq 50ns) ** Under Bias

TRUTH TABLE

CS	WE WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	X	Not Selected	I_{SB} , I_{SB1}	High Z	
L	Н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc	Din	Write Cycle

PIN ARRANGEMENT



■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V _{LH}	2.4	3.5	6.0	V
	VIL	-0.3*		0.8	V

^{*} V_{IL} min=-1.0V (Pulse width≤50ns)

DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V\pm10\%$, GND=0V, $T_a=0$ to $+70^{\circ}$ C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5$ V, $V_{is} = GND$ to V_{CC}	_	_	2.0	μA
Output Leakage Current	I _{LO}	$\overline{\text{CS}} = V_{lH}, \ V_{l/0} = \text{GND to } V_{cc}$		_	2.0	μA
O	Icc	$\overline{\text{CS}} = V_{IL}, I_{I \sim 0} = 0 \text{mA}$	_	35	80	mA
Operating Power Supply Current -	Icci	$\overline{\text{CS}} = V_{IL}$, Minimum Cycle, Duty=100%, $I_{I \times O}$ =0mA	-	40	80	mA
Average Operating Current	Iccz**	Cycle=150ns, Duty=50%, I _{1/0} =0mA	-	35	_	mA
C. II D. C. I C.	I_{SB}	$\overline{\text{CS}} = V_{IH}$	_	5	12	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{in} \le 0.2 \text{V} \text{ or } V_{in} \ge V_{cc} - 0.2 \text{V}$	_	20	800	μA
O V .	Vol	I _{0L} =8mA	_	_	0.4	V
Output Voltage	V_{OH}	$I_{OH} = -3.2 \text{mA}$	2.4	_	_	V

Notes) * Typical limits are at $V_{\rm CC} = 5.0 \, \rm V$, $Ta = 25 \, \rm ^{\circ} C$ and specified loading. ** Reference only.

ECAPACITANCE ($Ta=25^{\circ}\text{C}$, f=1MHz)

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	Cin	V.,-0V	head I	5	pF
Input/Output Capacitance	C1/0	$V_{I \times O} = 0 \text{ V}$	_	12	pF

Note) This parameter is sampled and not 100% tested.

MAC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_{a} = 0$ to $+70^{\circ}$ C, unless otherwise noted)

• AC TEST CONDITIONS

TREAD CYCLE

Input Pulse Levels GND to 3.0V Input Rise and Fall Times 10ns Input and Output Timing Reference Levels 1.5V Output Load See Figure 1



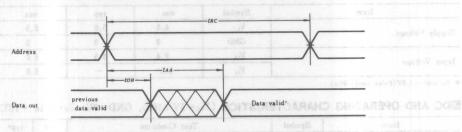
\$510Ω 5pF

Fig. 1

Parameter	Combal	HM61	48/P	HM614	17.1	
	Symbol	min	max	min	max	Unit
Read Cycle Time	t _{RC}	70	_	85	_	ns
Address Access Time	taa	_	70	_	85	ns
Chip Select Access Time	tacs	_	70	_	85	ns
Output Hold from Address Change	t OH	5	_	5	-	ns
Chip Selection to Output in Low Z*	t _{LZ}	10	_	10	_	ns
Chip Deselection to Output in High Z*	t _{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t _{PU}	0	_	0	_	ns
Chip Deselection to Power Down Time	tpD	_	40	_	40	ns

^{*} Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2) BHOFFIGHOO BHITARBED CO GROWINGOER R

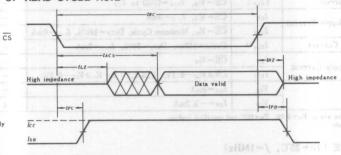


TIMING WAVEFORM OF READ CYCLE NO.2(1)(3)

Data out

Vcc supply

current



- NOTES) 1. WE is high for Read Cycle.
 - 2. Device is continuously selected, CS = VIL
 - 3. Address Valid prior to or coincident with CS transition low.

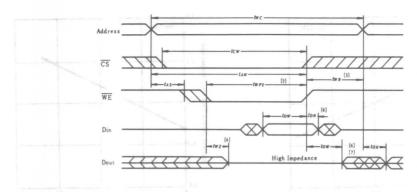
WRITE CYCLE

Parameter	Symbol	HM6	148/P	HM614	18/P-6	Unit
rarameter	Symbol	min	max	min	max	onit oceat Pulsa to
Write Cycle Time	twc	70		85	: - + 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ns ns
Chip Selection to End of Write	tcw	50		60	A premit tug	ns
Address Valid to End of Write	taw	65	*****	80		ns
Address Setup Time	tas	15	-	15	HEATING SHOP	ns
W. D. Wills	twp1	50	-	60	_	ns
Write Pulse Width®	twp2	65		80	_	ns
Write Recovery Time	tw _R	5	-	5	_	ns
Data Valid to End of Write	t _{DW}	30	-	35	8 871	ns
Data Hold Time	t _{DH}	5	-	5	_	ns
Write Enabled to Output in High Z**	twz	0	35	0	45	ns
Output Active from End of Write**	tow	0	_	0	- HJ0	ns

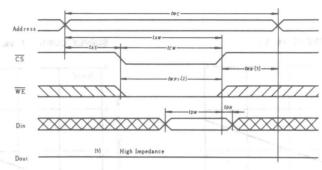
Notes) * When the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition. I/O pins remain in a high impedance state. In this case t_{WP1} , in the other case $t_{WP1} (-t_{WZ} + t_{DW})$.

** Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO.1(WE CONTROLLED) (1)



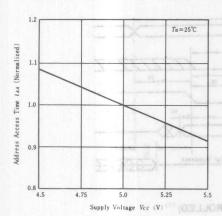
● TIMING WAVEFORM OF WRITE CYCLE NO.2(CS CONTROLLED) (1)



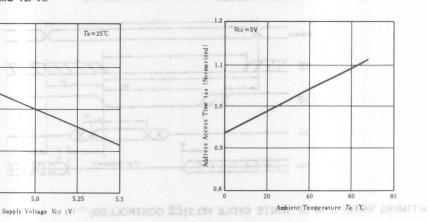
Notes)

- 1. $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are paced in the WRITE state during low level period
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$. (t_{WP})
- t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
- 4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain in a high impedance state.
- If CS is low during this period, I/O pins are in the output state.
 Then the data input signals of opposite phase to the outputs must not be applied to them.
- 7. Dout is the same phase of write data of this write cycle.

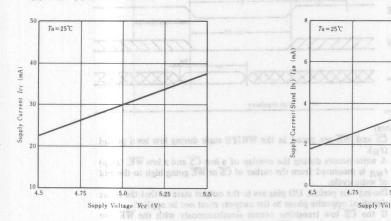
ACCESS TIME VS. Vcc



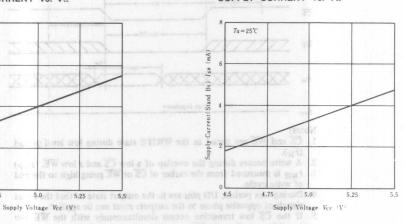
GRAJOATAGO SWALCA ACCESS TIME VS. Ta

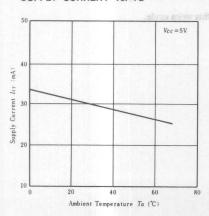


SUPPLY CURRENT vs. Vcc



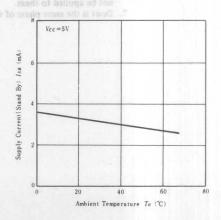
SUPPLY CURRENT vs. Vcc



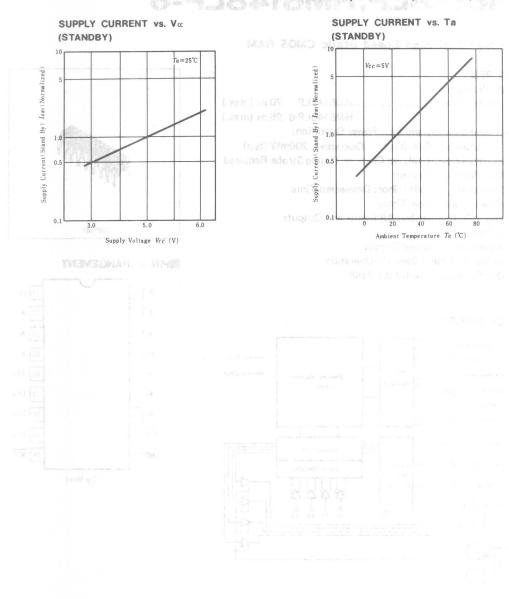


high impedence stars.

6. If CS is low during this period, 1/O pins are in the output state. SUPPLY CURRENT vs. Ta







HM6148LP, HM6148LP-6

1024-word×4-bit High Speed Static CMOS RAM

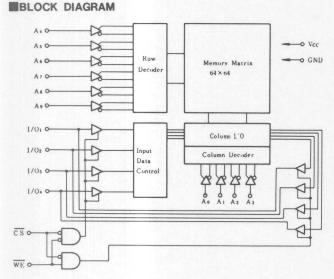
FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation;

Standby: 5µW (typ) Operation: 200mW (typ)

- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Capability of Battery Back Up Operation
- Pin-Out Compatible with Intel 2148

TOLOGK DIAGRAM

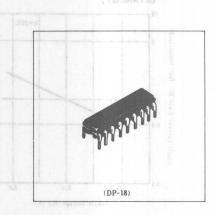


MADE AND LINE MAXIMUM RATINGS

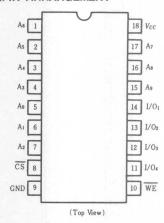
Item	Symbol	Value	Unit
Terminal Voltage*	V_T	-0.5△to +7.0	V
Power Dissipation	P_{T}	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tets	-55 to +125	°C
Storage Temperature**	Tota (bias)	-10 to +85	°C

^{*} with respect to GND. \triangle -1.0V (Pulse Width \leq 50ns)

** Under Bias



PIN ARRANGEMENT



TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not Selected	I_{SB} , I_{SB1}	High Z	
L	Н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc	Din	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

	Item	Symbol	(min	typ	max	Unit
Supply Voltage	Vcc	0 4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input Voltage		V_{IH}	2.4	3.5	6.0	V
		VIL	-0.3*	a monte a se	0.8	V V

^{*} V_{IL} min=-1.0V (Pulse width≤50ns)

DC AND OPERATING CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, GND=0V, $T_a = 0$ to $+70^{\circ}$ C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{L1} $	$V_{cc} = 5.5 \text{V}$, $V_{in} = \text{GND to } V_{cc}$		_	2.0	μΑ
Output Leakage Current	I _{LO}	$\overline{\text{CS}} = V_{IH}$, $V_{L/O} = \text{GND to } V_{CC}$	_	_	2.0	μΑ
Operating Power Supply Current	Icc	$\overline{\text{CS}} = V_{IL}, I_{LO} = 0 \text{mA}$	_	35	80	mA
Average Operating Current	Icci	$\overline{\text{CS}} = V_{IL}$, Minimum Cycle, Duty = 100%, $I_{LO} = 0$ mA	_	40	80	mA
	Iccz**	Cycle=150ns, Duty=50%, I _{1/0} =0mA	_	35	_	mA
C. II D. C. I C.	I_{SB}	$\overline{\text{CS}} = V_{IH}$	_	5	12	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{in} \le 0.2 \text{V} \text{ or } V_{in} \ge V_{cc} - 0.2 \text{V}$	_	1	100	μΑ
Output Voltage	Vol	$I_{OL} = 8 \text{mA}$	_	_	0.4	V
	Von	$I_{OH} = -3.2 \text{mA}$	2.4	_	_	V

Notes) * Typical limits are at $V_{\rm CC} = 5.0 \, \rm V$, $Ta = 25 \, \rm ^{\circ} C$ and specified loading.

ECAPACITANCE $(Ta=25^{\circ}\text{C}, f=1\text{MHz})$

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	C_{in}	V., = 0 V	_	5	pF
Input/Output Capacitance	C _{1.0}	$V_{I \sim 0} = 0 \text{ V}$	_ ****	12	pF

Note) This parameter is sampled and not 100% tested.

BAC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=0$ to $+70^{\circ}$ C, unless otherwise noted)

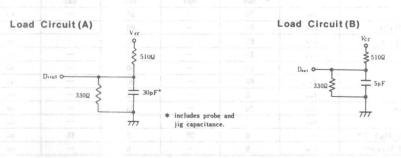
AC TEST CONDITIONS

 Input Pulse Levels
 GND to 3.0V

 Input Rise and Fall Times
 10ns

 Input and Output Timing Reference Levels
 1.5V

 Output Load
 See Figure



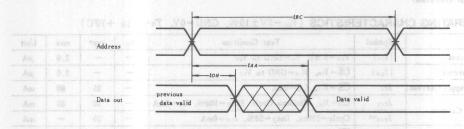
^{**} Reference only.

• READ CYCLE

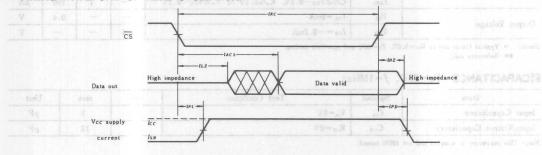
I/O Pin Reference Cycle	0 1 1	HM6148LP		HM61	HM6148LP-6	
Parameter S. Auth	Symbol	min l	max	Min min	max	Unit
Read Cycle Time	trc	70		85	- T	ns
Address Access Time	tan	201	70	SI-10	85	ns
Chip Select Access Time	tacs	tylin mente d <u>ad</u> er som	70		85	ns
Output Hold from Address Change	toн	5	a language and	5	La a managara	ns
Chip Selection to Output in Low Z*	tLZ	10	OFFICE OF F	10	TURKA SECRETARI	ns
Chip Deselection to Output in High Z*	tHZ	min 0	1004 40	0	40	ns
Chip Selection to Power Up Time	tpu	0	- Vco	0		ns
Chip Deselection to Power Down Time	tpD	0 -1	40	-	40	ns

* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF READ CYCLE NO.1 (1) (2)



TIMING WAVEFORM OF READ CYCLE NO.2(1)(3)



NOTES) 1. WE is high for Read Cycle.

2. Device is continuously selected, CS = V_{IL}

3. Address Valid prior to or coincident with CS transition low.

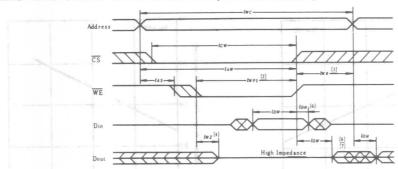
• WRITE CYCLE

Parameter	C	HM6148LP		HM6	HM6148LP-6		
rarameter	Symbol	min	max	min	max	be Unit	
Write Cycle Time	twc	70	_	85		ns	
Chip Selection to End of Write	tcw	50		60	(v) Hearig	ns	
Address Valid to End of Write	taw	65	_	80	I	ns	
Address Setup Time	tas	15	_	15	-	ns	
Write Pulse Width*	twp1	50	-	60		ns	
	twp2	65	_	80		ns	
Write Recovery Time	tw _R	5	_	5	S 2014-	ns	
Data Valid to End of Write	tow	30	-	35	-	ns	
Data Hold Time	t _{DH}	5	108/108015 51	5	_	ns	
Write Enabled to Output in High Z**	t wz	0	35	0	45	ns	
Output Active from End of Write**	tow	0	-	0		ns	

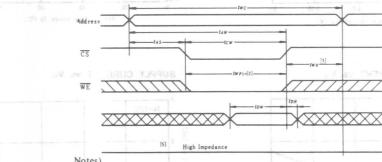
Notes) * When the CS low transition occurs simultaneously with the WE low transition or after the WE transition, I/O pins remain in a high impedance state. In this case t_{WP1} , in the other case $t_{WP2} (= t_{WZ} + t_{DW})$.

** Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1(WE CONTROLLED)(1)



● TIMING WAVEFORM OF WRITE CYCLE NO.2(CS CONTROLLED) (1)



Notes)

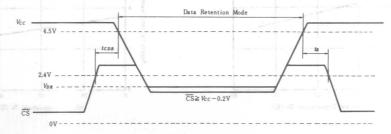
- 1. CS and WE are paced in the WRITE state during low level period
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$. (t_{WP}) 3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
- 4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 5. If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain in a high impedance state.
- 6. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
- 7. Dout is the same phase of write data of this write cycle.

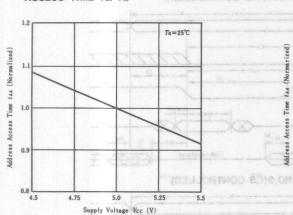
LOW V_{cc} DATA RETENTION CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, V_{in} \ge V_{CC} - 0.2 \text{V} \text{ or } V_{in} \le 0.2 \text{V}$	2.0	-	_	V
Data Retention Current	ICCDR	$V_{CC} = 2.0 \text{ V}, \ \overline{\text{CS}} \ge 1.8 \text{ V}, \ V_{in} = 1.8 \text{ V} \text{ or } V_{in} \le 0.2 \text{ V}$	_	-	40	μA
Chip Deselect to Data Retention Time	tcor	C. D W. (0	-	_	ns
Operation Recovery Time	t _R	See Retention Waveform		_	_	ns

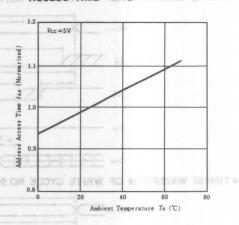
^{*} tRC - Read Cycle Time

● LOW Vcc DATA RETENTION WAVEFORM

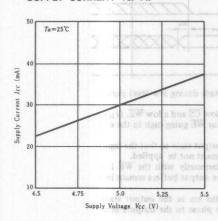




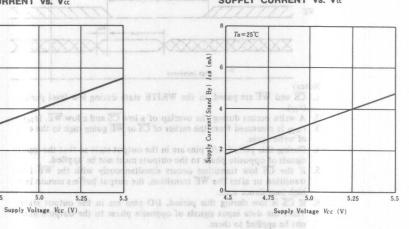
ACCESS TIME VS. Va ACCESS TIME VS. Ta ROTENAM ON MATE



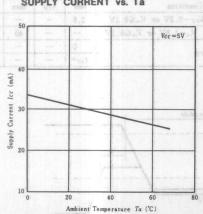
SUPPLY CURRENT vs. Vcc



SUPPLY CURRENT vs. Va

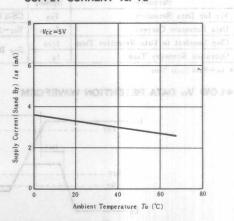


SUPPLY CURRENT vs. Ta

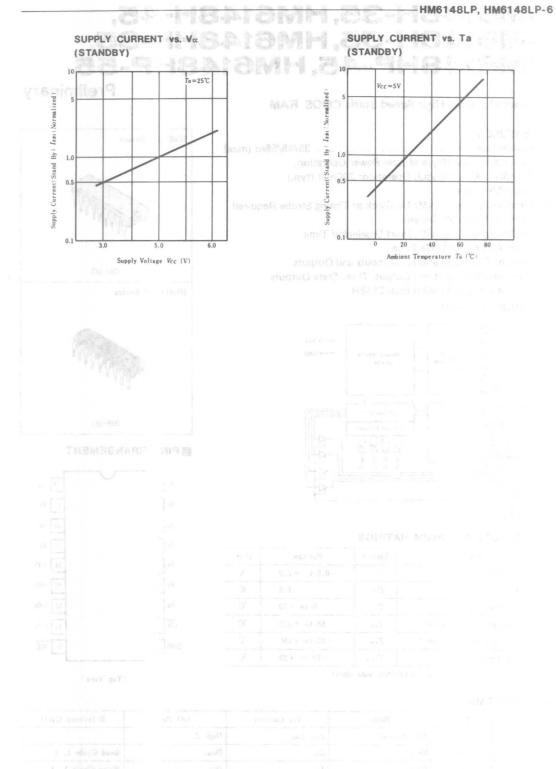


SUPPLY CURRENT vs. Ta

BLOW Ve DATA RETENTION CHARACTERISTICS (74-8 to +700)



Dout is the same place of write data of this write cycle.



HM6148H-35, HM6148H-45, HM6148H-55, HM6148HP-35, HM6148HP-45, HM6148HP-55

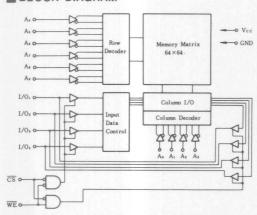
Preliminary

1024-word x 4-bit High Speed Static CMOS RAM

FEATURES

- Low Power Standby and Low Power Operation;
 Standby: 100 µW (typ.), Operation: 200mW (typ.)
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Common Data Input and Output; Three-State Outputs
- Pin-Out Compatible with Intel 2148H

■ BLOCK DIAGRAM



MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage*	V _T	-0.5 to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature (Plastic)	Tota	-55 to +125	°C
Storage Temperature (Ceramic)	Tstg	-65 to $+150$	°C
Storage Temperature**	Thias	-10 to +85	°C

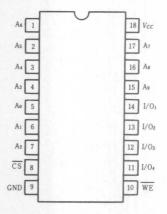
* with respect to GND.

 $V_{IL min} = -3.5 \text{ V} \text{ (Pulse width} = 20 \text{ ns)}$

* * under bias

(DG-18) HM6148HP Series (DP-18)

PIN ARRANGEMENT



(Top View)

TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not selected	IsB, IsB1	High Z	
L	Н	Read	Icc	Dout	Read Cycle 1, 2
L	L	Write	Icc	Din	Write Cycle 1, 2

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
66-9	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-68	6.0	V
	VIL	-0.5*	-	0.8	V

^{* -3.0} V (Pulse width 20 ns)

DC AND OPERATING CHARACTERISTICS[1] ($Ta=0\sim70^{\circ}\text{C}$, $V_{cc}=5\text{V}\pm10\%$, GND=0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	$ I_{L1} $	V_{CC} = max, V_{in} = GND to V_{CC}	-	-	2.0	μА	
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{I \times 0} = \text{GND to } V_{CC}$		-	2.0	μА	
Operating Power Supply Current	Icc	$\overline{\mathrm{CS}} = V_{IL}, I_{I \wedge O} = 0 \mathrm{mA}$		35	80	mA	
Operating Power Supply Current: AC	Icci	min. cycle, $\overline{CS} = V_{IL}, I_{I \times O} = 0$ mA	10 To	50	100	mA	(2)
Standby Power Supply Current: DC	I_{SB}	$\overline{\text{CS}} = V_{IH}$	-	5	20	mA	
Standby Power Supply Current(1): DC	I_{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, V_{IN} \le 0.2 \text{V} \text{ or}$ $V_{IN} \ge V_{CC} - 0.2 \text{V}$	87 <u>57</u> 4	20	800	μА	
Output Low Voltage	Vol	IoL=8mA	_	_	0.4	V	
Output High Voltage	V_{OH}	$I_{OH} = -4.0 \text{mA}$	2.4	_	_	V	

Notes) 1. Typical limits are at V_{cc} =5.0V, Ta=+25°C and specified loading. 2. 120mA max. for HM6148HP-35

CAPACITANCE $(Ta=25 \,^{\circ}\text{C}, f=1 \,^{\circ}\text{MHz})$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	V = 0 V	3	5	pF
Input/Output Capacitance	C1/0	V _{1 × 0} = 0 V	5	7	pF

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS $(V_{cc}=5V\pm10\%, Ta=0 \text{ to } +70^{\circ}\text{C})$

•RISE FALL TIME

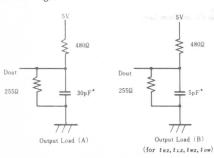
Item	Symbol	min	typ	max	Unit
Input Rise Time	t,	-	5	100	ns
Input Fall Time	- t ₁	\ \ \ — = = = = = = = = = = = = = = = =	5 5	100	ns

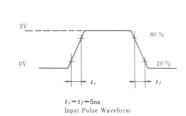
•AC TEST CONDITIONS

Input pulse levels: GND to 3.0V Input rise and fall times: 5ns

Input and Output timing reference levels: 1.5V

Output load: See Figure





* Including scope & jig.

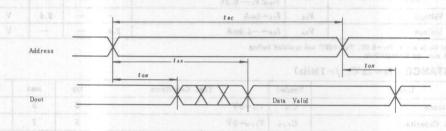


BAC CHARACTERISTICS (Ta=0 to 70°C, $V_{cc}=5V\pm10\%$, unless otherwise noted.) • READ CYCLE

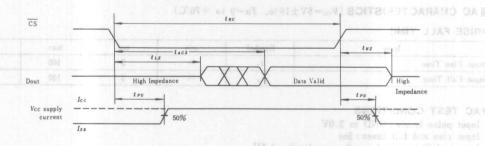
	Cb.l	HM614	8HP-35	HM6148	HP-45	HM6148HP-55		I I-:a
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	t _{RC}	35	70.0	45	8.8	55	-	ns
Address Access Time	tAA	y	35	-	45	-	55	ns
Chip Select Access Time	tACS	-	35	_	45	-	55	ns
Output Hold from Address Change	t _{OH}	5	_	5	_	5	- 1	ns
Chip Selection to Output in Low Z	t _{LZ} *	10	10 7118	10	MARO	10	170 O	ns
Chip Deselection to Output in High Z	t _{HZ} *	ibno o les	20	0	20	0	20	ns
Chip Selection to Power Up Time	t _{PU}	0	,33M=55	0		0	sge Carre	ns
Chip Deselection to Power Down Time	t _{PD}	300	30	1937	30	10	30	ns

^{*} Transition is measured ±500 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested. At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



Notes) 1. \overline{WE} is High for Read Cycle.

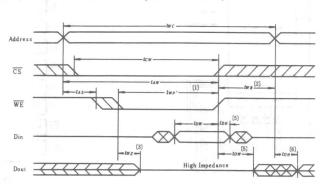
Device is continuously selected, CS = V_{IL}.
 Address Valid prior to or coincident with CS transition Low.

• WRITE CYCLE

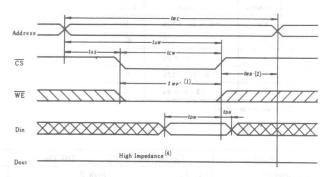
Terror	C 11	HM614	18H/P-35	HM6148	H/P-45	HM6148	BH/P-55	V TT-14
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	35		45		55		ns
Chip Selection to End of Write	tcw	30	Divis)	40	eo Tar	50	A	ns
Address Valid to End of Write	t _{AW}	30	_	40) 2 0 8V.	50	-,,,	ns
Address Setup Time	tas	0	_	no d 0100	J Q U Ab	0	- 1	ns
Write Pulse Width	twp	30	_	35	_	40	_	ns
Write Recovery Time	twr	5) (m)ng is	5	01 <u>0</u>	5	_	ns
Data Valid to End of Write	t _{DW}	20	_	20	_	20	_	ns
Data Hold Time	t _{DH}	0	emiT	0.0	3 JT 17	0	700	ns
Write Enabled to Output in High Z*	twz	0	10	0	15	0	20	ns
Output Active from End of Write*	t ow	0	Qu tt auts	0 110	3 V 3	0	_	ns

^{*} Transition is measured ±500 mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO.2 (CS Controlled)



NOTES of Timing Waveform of Write

- of liming Waveform of Write

 1. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$. (t_{wp})

 2. t_{wp} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.

 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

 4. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition, the output buffers remain
- in a high impedance state.

 5. If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

 6. Dout is the same phase of write data of this
- write cycle.



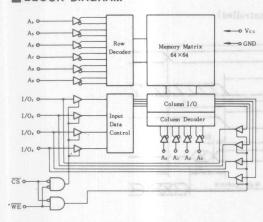
HM6148HLP-35, HM6148HLP-45, HM6148HLP-55 Preliminary

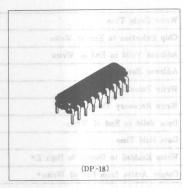
1024-word × 4-bit High Speed Static CMOS RAM

FEATURES

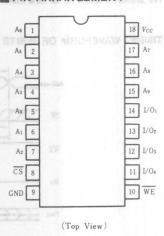
- Low Power Standby and Low Power Operation; Standby: 5μW (typ.), Operation: 300mW (typ.)
- Fast Access Time: 35/45/55ns (max)
- Capability of Battery Back Up Operation
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of tacs with Short Deselected Time
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Three State Output
- Pin-Out Compatible with Intel 2148H

BLOCK DIAGRAM





PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage*	V _T ·	-0.5 to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C
Storage Temperature **	Thies	-10 to +85	°C

^{*} with respect to GND.

* * under bias.

TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not selected	IsB, IsB1	High Z	
L	Н	Read	Icc (ant) AW not a	Dout A server at a	Read Cycle 1, 2
L	AsiaL at me	Write was a second at a	Icc	Din	Write Cycle 1, 2

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.

 $V_{IL min} = -3.5 \text{ V} \text{ (Pulse width} = 20 \text{ ns)}$

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
#-9.11	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	<u>a</u>	6.0	V
	V_{IL}	-0.5 *	=	0.8	V

^{* -3.0} V (Pulse width 20 ns)

DC AND OPERATING CHARACTERISTICS[1] $(Ta=0\sim70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, \text{GND}=0\text{V})$

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	I _{L1}	$V_{CC} = \max_{i} V_{in} = GND$ to V_{CC}	-	1 7	2.0	μΑ	
Output Leakage Current	ILO	$\overline{CS} = V_{IH}, V_{I \wedge O} = GND$ to V_{CC}	um I A		2.0	μА	
Operating Power Supply Current: DC	Icc	$\overline{CS} = V_{IL}, I_{I \neq O} = 0 \text{mA}$		35	80	mA	
Operating Power Supply Current: AC	Icc1	min. cycle, $\overline{CS} = V_{IL}$, $I_{I \times 0} = 0$ mA	- 5± <u>-</u> 4±	50	100	mA	(2)
Standby Power Supply Current: DC	I_{SB}	$\overline{CS} = V_{IH}$	_	5	20	mA	
Standby Power Supply Current(1): DC	I_{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, V_{IN} \le 0.2 \text{V} \text{ or}$ $V_{IN} \ge V_{CC} - 0.2 \text{V}$	Aug -	1	50	μΑ	-
Output Low Voltage	Vol	$I_{OL} = 8 \text{mA}$	_	_	0.4	V	
Output High Voltage	Von	$I_{OH} = -4.0 \text{mA}$	2.4	7—	_	V	

Notes) 1. Typical limits are at $V_{\rm CC}$ =5.0V, Ta=+25°C and specified loading. 2. 120mA max. for HM6148HLP-35

CAPACITANCE $(Ta=25 \, ^{\circ}\text{C}, f=1 \, \text{MHz})$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	C1/0	$V_{I \times O} = 0 \text{ V}$	5	7	pF

Note) This parameter is sampled and not $100\,\%$ tested.

AC CHARACTERISTICS $(V_{cc}=5V\pm10\%, T_a=0 \text{ to } +70^{\circ}\text{C})$

•RISE FALL TIME

Item	Symbol	min	typ	max	Uniț
Input Rise Time	t,		5	100	ns
Input Fall Time	t,	773	5	100	ns

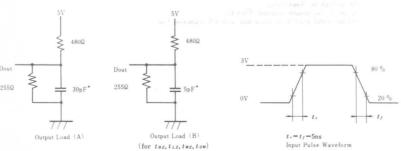
•AC TEST CONDITIONS

Input pulse levels: GND to 3.0V

Input rise and fall times: 5ns

Input and Output timing reference levels: 1.5V

Output load: See Figure



* Including scope & jig.



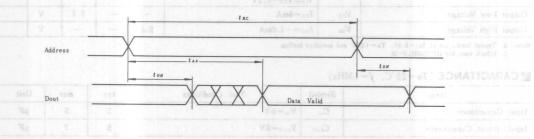
HM6148HLP-35, HM6148HLP-45, HM6148HLP-55

BAC CHARACTERISTICS (Ta=0 to 70°C, $V_{CC}=5V\pm10\%$, unless otherwise noted.) • READ CYCLE

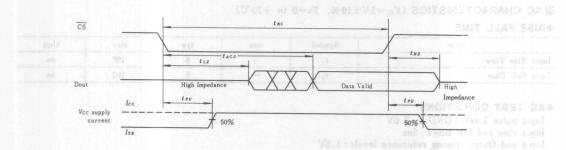
	1.00		750		-		
C1-1	HM614	8HLP-35	HM6148	HLP-45	15 HM6148HLP-5		Unit
Symbol	min	max	min	max	min	max	Unit
tRC	35	0.8	45	8.78	55	-	ns
tAA	7	35	-	45	- T	55	ns
tacs	-	35	-	45	- (1c	55	ns
t _{OH}	5	-	5	-	5	-	ns
t _{LZ} *	10	JE OLTE	10	RAHO	10	RACT GN	ns
t _{HZ} *	0	20	0.0	20	0	20	ns
t _{PU}	0	V _c , water, N	0	_	0	N 10 1 120	ns
t _{PD}	TMD-0.	30	1001	30	_ lns	30	ns
	tAA tACS tOH tLZ* tHZ*	Symbol min tRC 35 tAA — tACS — tOH 5 tLZ* 10 tHZ* 0 tPU 0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Symbol min max min t_{RC} 35 - 45 t_{AA} - 35 - t_{ACS} - 35 - t_{OH} 5 - 5 t_{LZ}^* 10 - 10 t_{HZ}^* 0 20 0 t_{PV} 0 - 0	Symbol min max min max t_{RC} 35 - 45 - t_{AA} - 35 - 45 t_{ACS} - 35 - 45 t_{OH} 5 - 5 - t_{LZ}^* 10 - 10 - t_{HZ}^* 0 20 0 20 t_{PV} 0 - 0 -	Symbol min max min max min t_{RC} 35 - 45 - 55 t_{AA} - 35 - 45 - t_{ACS} - 35 - 45 - t_{OH} 5 - 5 - 5 t_{LL}^* 10 - 10 - 10 t_{HZ}^* 0 20 0 20 0 t_{PU} 0 - 0 - 0	Symbol min max min max min max t_{RC} 35 - 45 - 55 - t_{AA} - 35 - 45 - 55 t_{ACS} - 35 - 45 - 55 t_{OH} 5 - 5 - 5 - t_{LZ} 10 - 10 - 10 - t_{HZ} 0 20 0 20 0 20 t_{PV} 0 - 0 - 0 -

^{*} Transition is measured ±500 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested. At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



- Notes) 1. WE is High for Read Cycle.

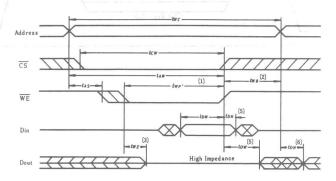
 - Device is continuously selected, S = V_{IL}.
 Address Valid prior to or coincident with S transition Low.

• WRITE CYCLE

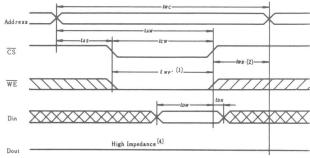
Item 100	Symbol	HM6148	HLP-35	HM6148	HLP-45	HM6148	HLP-55	Unit
Item	Symbol	min	max	min	max	min	max	
Write Cycle Time	twc	35	N = 20	45	_	55	_	ns
Chip Selection to End of Write	t av	30	NA VO	40		50	_	ns
Address Valid to End of Write	t av	30	4 ≤70	40	327	50	_	ns
Address Setup Time	tas	0		0		- 0	_	ns
Write Pulse Width	twp	30	_	35	· · ·	40		ns
Write Recovery Time	t _{wr}	5	_	5	_	5	_	ns
Data Valid to End of Write	t _{DW}	20		20		20	_	ns
Data Hold Time	t _{DH}	0	- ****	0	- 201 41	0	_	ns
Write Enabled to Output in High Z*	twz	0	10	0	15	0	20	ns
Output Active from End of Write*	tow 40	0	m x = 1.	0		0	_	ns

* Transition is measured ±500 mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested. All inputs t_r , t_f (rise and fall time) are less than 100 ns.

• TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO.2 (CS Controlled)



Notes of Timing Waveform of Write

Notes of Timing Waveform of Write:

1. A write occurs during the overlap of the low CS and a low WE. (twp)

2. twa is measured from the earlier of CS or WE going high to the end of write cycle.

3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

4. If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain in a high impedance state.

5. If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

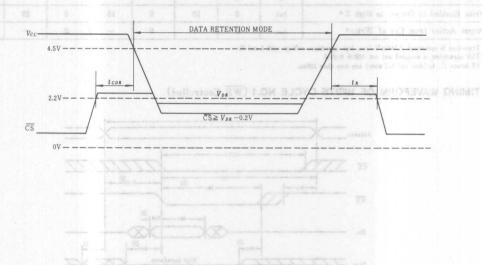
6. Dout is the same phase of write data of this write cycle.

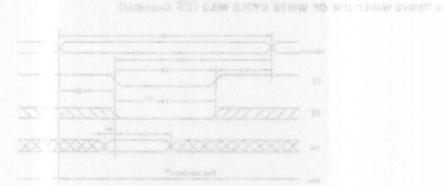
LOW V_{cc} DATA RETENTION CHARACTERISTICS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDR	xon ele	2.0			V
Data Retention Current	,	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V}$			30*	A
Data Retention Current	ICCDR	$V_{in} \ge V_{cc} - 0.2 \text{V}$ or	443	all to he	20**	μΑ
Chip Deselect to Data Retention Time	tcor	$0 \stackrel{\vee}{V} \leq V_{in} \leq 0.2 \stackrel{\vee}{V}$	0	HORE YOU I	Total State	ns
Operation Recovery Time	t _R		t _{RC (1)}		77 - 27	ns

Note) 1. t_{RC} =Read Cycle Time. $*V_{CC}$ =3.0V $**V_{CC}$ =2.0V

OLOW VCC DATA RETENTION WAVEFORM





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L. A whice course sharing the William of St. and S. See W. St. and

L. A whice course sharing the constant of the C.S. can W.S. going high to the could set write coulde.

S. Dering this percent, U.C. are a recommendation of the constant of a cipacity of appearance of the original state on the charing the coupled and the original set of a constant of the coupled with the W.E. can be counted by M.E. C. B. C. S. See the counter of the coupled by the coupled of the coupled or the coupled by the coupled of the coupled or the coupled or

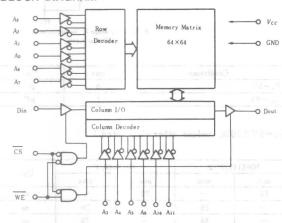
HM6147, HM6147-3 HM6147P, HM6147P-3

4096-word×1-bit High Speed Static CMOS RAM

FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby:100μW typ., Operation: 75mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

BLOCK DIAGRAM



MADE ADSOLUTE MAXIMUM RATINGS

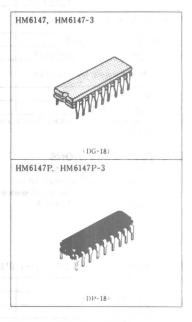
Item 0	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature(Ceramic)	Tate	-65 to +150	°C
Storage Temperature(Plastic)	Tstg	-55 to +125	°C

^{*} $V_{IN} \min = -1.0 \text{V (Pulse Width} \leq 20 \text{ns})$

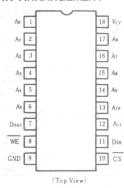
PRECOMMENDED DC OPERATING CONDITIONS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
en 0	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	- O	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	VIL	-0.3*		0.8	V

^{*} $V_{IL} \min = -1.0 \text{V} \text{ (Pulse width} \leq 20 \text{ns} \text{)}$



PIN ARRANGEMENT



DC AND OPERATING CHARACTERISTICS (0°C $\leq Ta \leq 70$ °C, $V_{cc} = 5V \pm 10\%$, GND=0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	$ I_{LI} $	Vcc=5.5V, GND to Vcc	_	_	2.0	μΑ	
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{\text{out}} = 0 \sim V_{\text{CC}}$	baen	i doll	2.0	μΑ	Lapn
Operating Power Supply Current(1) DC	Icc	$\overline{\mathrm{CS}} = V_{IL}$, Output open	_	15	35	mA	
Operating Power Supply Current(2) DC	Iccı	$\overline{\text{CS}} = V_{IL}, \ V_{IN} \le 0.2 \text{V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{V}$	-	12	- I don't	mA	(2)
Average Operating Current(3)	Iccz	Cycle 150ns, duty 50%		14		mA	(2)
Standby Power Supply Current(1) DC	IsB	$\overline{\mathrm{CS}} = V_{IH}$	-	5	12	mA	1.08177
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2\text{V},$ $V_{IN} \le 0.2\text{V or } V_{IN} \ge V_{CC} - 0.2\text{V}$	inobat	20	800	μΑ	Stans
Output Low Voltage	Vol	$I_{oL} = 12 \text{mA}$	- A	O PO TO A S	0.40	V	MIOO
Output High Voltage	VoH	$I_{OH} = -8.0 \text{mA}$	2.4	-	_	V	0.0673

Note) 1. Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

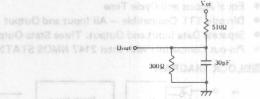
2. Reference only

MAC TEST CONDITIONS

Input pulse levels: GND to 3.5V
 Input rise and fall times: 10 ns

Input and output timing reference levels: 1.5V

Output load: See Figure 1



* Including scope & jig capacitance Figure 1 Output Load

ECAPACITANCE ($Ta=25^{\circ}C$, f=1.0 MHz)

Item	Item Symbol Conditions		max	Unit
Input Capacitance	Cin	V _{in} =0V	5 - 0	pF
Output Capacitance	Cout	Vout = 0V	7	pF

Note) This parameter is sampled and not 100% tested.

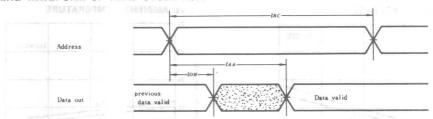
MAC CHARACTERISTICS ($Ta=0^{\circ}\text{C}$ to 70°C , $V_{cc}=5\text{V}\pm10\%$, unless otherwise noted.) • READ CYCLE

Parameter	Symbol	HM614	HM6147/P-3		6147/P	Unit
rarameter	Symbol	min	max	min	max	Onit
Read Cycle Time	tRC	55	_	70	1 - 0	ns
Address Access Time	taa	-	55	0 0 0 0	70	ns
Chip Select Access Time	tacs	-	55	_	70	ns
Output Hold from Address Change	t _{OH}	5	-	5		ns
Chip Selection to Output in Low Z	tLZ	10	_	10	SHICKNITE THE THE	ns
Chip Deselection to Output in High Z	tHZ	0	40	lorimy 0	40	ns
Chip Selection to Power Up Time	t _{PU}	7.0 0	os d .0 -	0	* Web or Totales a 9	ns
Chip Deselection to Power Down Time	t _{PD}	7 0 1	30		30	ns

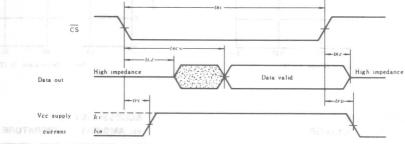
• WRITE CYCLE

Parameter	Combal	HM6	147/P-3	HM6	147/P	Tiris
rarameter	Symbol	min	max	min	max	Unit
Write Cycle Time	twc	55	-	70		ns
Chip Selection to End of Write	tcw	45	COMBITION	55	Mon THO	ns
Address Valid to End of Write	t _A w	45	lasks; cc	55	Crec-Trans	ns
Address Setup Time	tas	0	-	0	_	ns
Write Pulse Width	twp	35	mes	40	_	ns qua
Write Recovery Time	twR	10	-	15		ns
Data Valid to End of Write	tow	25	<u> </u>	30	9890.15. (1.3)	ns
Data Hold Time	t _{DH}	10	23	10	1866 (D.) VB. 0	ns
Write Enabled to Output in High Z	t wz	0	30	0	35	ns
Output Active from End of Write	tow	0	-	0	-	ns

● TIMING WAVEFORM OF READ CYCLE NO.1 (1) (2)



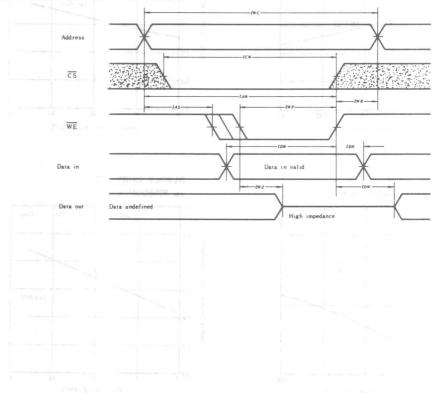
● TIMING WAVEFORM OF READ CYCLE NO.2(1)(3)



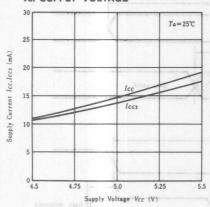
Notes: 1. WE is high for READ Cycle. 2. CS is low for READ Cycle.

3. Addresses valid prior to or coincident with CS transition low.

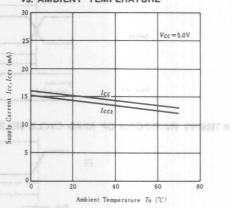
TIMING WAVEFORM OF WRITE CYCLE



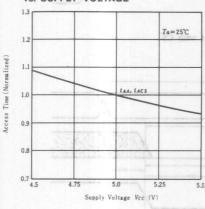
SUPPLY CURRENT vs. SUPPLY VOLTAGE



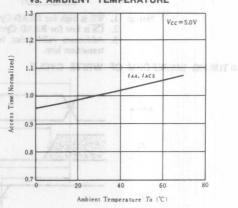
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



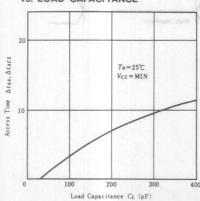
ACCESS TIME
vs. SUPPLY VOLTAGE



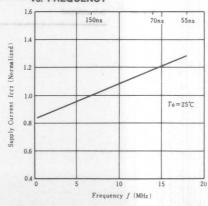
ACCESS TIME vs. AMBIENT TEMPERATURE



ACCESS TIME
vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. FREQUENCY



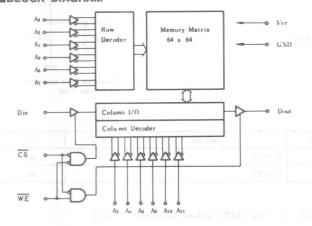
HM6147LP, HM6147LP-3

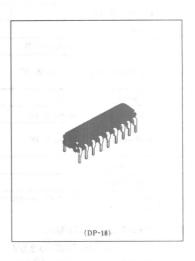
4096-word×1-bit High Speed Static CMOS RAM

FEATURES

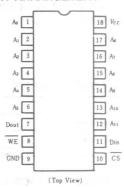
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 5μW typ. Operation: 75mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Capability of Battery Back up Operation
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

BLOCK DIAGRAM





PIN ARRANGEMENT



MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	Vτ	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tets	-55 to +125	°C

^{*} $V_{IL} \min = -1.0 \text{V (Pulse Width} \le 20 \text{ ns)}$

TRECOMMENDED DC OPERATING CONDITIONS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V _{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	VIL	-0.3*	_	0.8	V

^{*} V_{IL} min=-1.0V (Pulse width≤20ns)



DC AND OPERATING CHARACTERISTICS (0°C $\leq Ta \leq 70$ °C, $V_{CC} = 5V \pm 10\%$, GND=0V)

Parameter	Symbol	Test Condition	min	typ	max	Unit	Notes
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5$ V, GND to V_{cc}	-	-	2.0	μΑ	
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{out} = 0 \sim V_{CC}$	-	_	2.0	μΑ	MARI
Operating Power Supply Current(1) DC	Icc	$\overline{\mathrm{CS}} = V_{IL}$, Output open		15	35	mA	BYTEC 5
Operating Power Supply Current(2) DC	Icci	$\overline{\text{CS}} = V_{IL}, \ V_{IN} \leq 0.2 \text{V} \text{ or } V_{IN} \geq V_{CC} = 0.2 \text{V}$	o earin 19 1 4 0J	12	Services	mA	(2)
Average Operating Current(3)	Iccz	Cycle 150ns, duty 50%	- 7/16	14	iner a i	mA	(2)
Standby Power Supply Current(1) DC	I_{SB}	$\overline{\text{CS}} = V_{IH}$	-	5	12	mA	Flect
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, V_{IN} \le 0.2 \text{V} \text{ or}$ $V_{IN} \ge V_{CC} - 0.2 \text{V}$	ins Share C	muO n	100	μА	No.
Output Low Voltage	Vol	I _{OL} = 12mA	350	adelia az	0.40	V	1.07
Output High Voltage	V _{OH}	$I_{OH} = -8.0 \text{mA}$	2.4	bd5 11	on (att	V	ca2 a

C-TLIFF OF CHART, TLIFF ON CHIVING

Note) 1. Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

2. Reference only.

MAC TEST CONDITIONS

Input pulse levels: GND to 3.5V

Input rise and fall times: 10 ns

Input and output timing reference levels: 1.5V

Output load: See Figure 1



* Including scope & jig capacitance Figure 1 Output Load

EXAMPLE 1.0 CAPACITANCE $(Ta=25^{\circ}\text{C}, f=1.0\text{MHz})$

Item 1	Symbol	Condition	max	Unit	
Input Capacitance	Cin	$V_{IN}=0$ V	88888 5	pF	
Output Capacitance	Cont	$V_{out} = 0 \text{ V}$	7	pF	

Note) This parameter is sampled and not 100% tested.

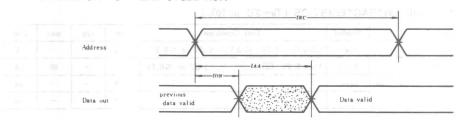
AC CHARACTERISTICS ($Ta=0^{\circ}$ C to 70° C, $V_{cc}=5V\pm10\%$, unless otherwise noted.) • **READ CYCLE**

Parameter	Symbol	HM61	47LP-3	HM61	Unit	
rarameter	Symbol	min	max	min	max	Unit
Read Cycle Time	tRC	55		70	w Pie - Line	ns
Address Access Time	taa	7 7	55	a -	70	ns
Chip Select Access Time	tacs		55	7 -	70	ns
Output Hold from Address Change	ton	5	38-4	5		ns
Chip Selection to Output in Low Z	tLZ	10	-	10	East / Hally Co	ns
Chip Deselection to Output in High Z	tHZ	0	40	0	40	ns
Chip Selection to Power Up Time	t _{PU}	0	_	0	-	ns
Chip Deselection to Power Down Time	tpp	-	30		30	ns

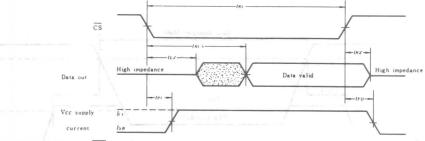
• WRITE CYCLE

D	C 1.1	HM61	47LP-3	HM61	47LP	Unit	
Parameter	Symbol	min	max	min	max	Unit	
Write Cycle Time	twc	55		70	_	ns	
Chip Selection to End of Write	tcw	45	_	55	_	ns	
Address Valid to End of Write	t _{AW}	45	- 1	55	_	ns	
Address Setup Time	tas	0	_	0	_	ns	
Write Pulse Width	t_{WP}	35		40	_	ns	
Write Recovery Time	t _{WR}	10	/-	15	_	ns	
Data Valid to End of Write	t _{DW}	25	_	30	_	ns	
Data Hold Time	t _{DH}	10	_	10	_	ns	
Write Enabled to Output in High Z	twz	0	30	0	35	ns	
Output Active from End of Write	tow	0		0	_	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1(1)(2)

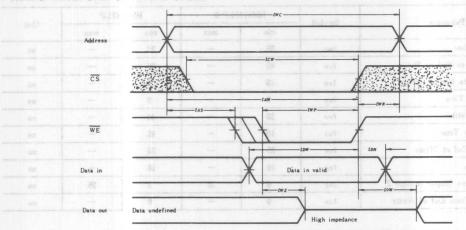


● TIMING WAVEFORM OF READ CYCLE NO.2(1)(3)



- NOTES: 1. WE is high for READ Cycle.
 2. CS is low for READ Cycle.
 3. Addresses valid prior to or coincident with CS transition low.

TIMING WAVEFORM OF WRITE CYCLE



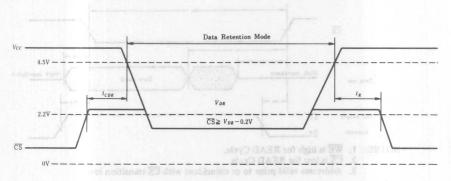
* WRITE CYCLE

■LOW V_{cc} RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, V_{in} \ge V_{CC} - 0.2 \text{V} \text{ or } \le 0.2 \text{V}$	2.0	111.20	-	V
Data Retention Current	ICCDR	$V_{cc}=2.0V$, $\overline{CS} \ge 1.8V$, $V_{in} \ge 1.8V$ or $\le 0.2V$	-	-	40	μА
Chip Deselect to Data Retention Time	tcor		0	_	-	ns
Operation Recovery Time	t _R	bitev grab	t _{RC} *		_	ns

^{*} tRC - Read Cycle Time

● LOW Vcc RETENTION CHARACTERISTICS



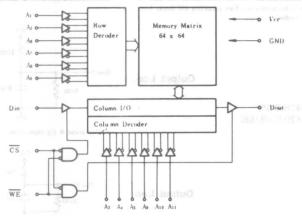
HM6147H-35, HM6147H-45, HM6147H-55, HM6147HP-35, HM6147HP-45, HM6147HP-55

4096-word×1-bit High Speed Static CMOS RAM

FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns/55ns Max.
- Low Power Standby and Low Power Operation, Standby: 100µW typ., Operation: 150mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM

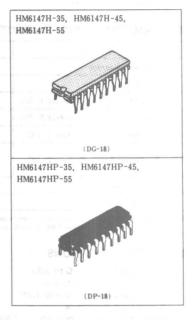
BLOCK DIAGRAM



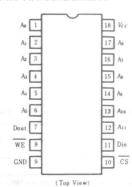
MADE ADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	Vτ	-3.5* to +7.0	V
DC Output Current	I .	20	m A
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	·°C
Storage Temperature (under bias)	Tota (bias)	-10 to +85	°C
Storage Temperature (Ceramic)	T_{sts}	-65 to +150	°C
Storage Temperature (Plastic)	Tets	-55 to +125	°C

^{*} Pulse Width 20ns, DC: -0.5V



MPIN ARRANGEMENT



TRECOMMENDED DC OPERATING COMDITIONS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	VIL	-3.0*	pred best	0.8	V

^{*} Pulse Width 20ns, DC: -0.5V

DC AND OPERATING CHARACTERISTICS (0°C $\leq Ta \leq 70$ °C, $V_{CC} = 5V \pm 10\%$, GND=0V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	Vcc=5.5V, GND to Vcc	ARCAL CRIN	yucosi V	10	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{\text{out}} = 0 \text{V} \sim V_{CC}$	1 - V30	mcM sice	10	μΑ
Operating Power Supply Current(1) DC	Icc	$\overline{CS} = V_{IL}$, Output open	_	30	80	mA
Operating Power Supply Current(2) DC	Icci	$\overline{CS} = V_{IL}$, Minimum Cycle	1 091	40	80	mA
Standby Power Supply Current(1) DC	I_{SB}	$\overline{\text{CS}} = V_{IH}, \ V_{CC} = \text{Min to Max}$	Bhort C	1097 8 NA	20	mA
Standby Power Supply Current (2) DC	I_{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V},$ $V_{IN} \le 0.2 \text{V}$ or $V_{IN} \ge V_{CC} - 0.2 \text{V}$	e —All I	20	800	μΑ
Output Low Voltage	Vol	IoL = 8mA	I leant di	ive atterns	0.40	V
Output High Voltage	Von	$I_{OH} = -4 \mathrm{mA}$	2.4	F A	0.56 <u>76</u> 1	V

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.

2. Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

MAC TEST CONDITIONS

Input pulse levels: GND to 3.0V

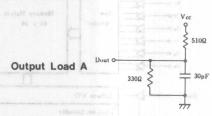
Input rise and fall times: 5 ns

Input timing reference levels: 1.5V

Output load: See Figure

Output timing reference levels: 1.5V (HM6147H/P-35)

0.8 to 2.0V (HM6147H/P-45/55)



* Including scope & jig capacitance

§ 510Ω Output Load B

ECAPACITANCE $(Ta=25^{\circ}C, f=1.0 \text{MHz})$

Item	Symbol	Conditions	max	Unit
Input Capacitance	Cin	Vin=0V + outsels -	on states at	ve pF
Output Capacitance	Cout	$V_{out} = 0 \text{V}$	6 19	maiD approx DC

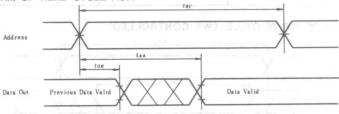
Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (Ta=0°C to 70°C, $Vcc=5V\pm10\%$, unless otherwise noted.)

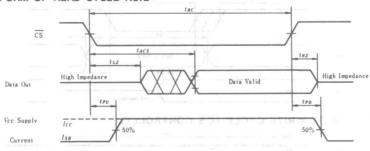
• READ CYCLE

asio? Sind P	C 11	HM6147H/P-35		HM6147H/P-45		HM6147H/P-55		Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Read Cycle Time	t _{RC}	35		45	+	55	_	ns	(1)
Address Access Time	tAA		35	-	45	-	55	ns	
Chip Select Access Time	tACS	-	35	-	45	_	55	ns	
Output Hold from Address Change	t _{OH}	5		5	10.0	5	_	ns	
Chip Selection to Output in Low Z	tLZ	5	_	5	_	5	_	ns	(2), (3), (7)
Chip Deselection to Output in High Z	t _{HZ}	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	t _{PU}	0		0	+	0	_	ns	
Chip Deselection to Power Down Time	t PD		20	-	20		20	ns	

TIMING WAVEFORM OF READ CYCLE NO.1 (4)(5)



TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)



- Notes: 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
 - 2. At any given temperature and voltage condition, tHZ max. is less than t_{LZ} min. both for a given device and from device to device.
 - 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

 WE is high for READ Cycle.

 Device is continuously selected, CS=V_{IL}.

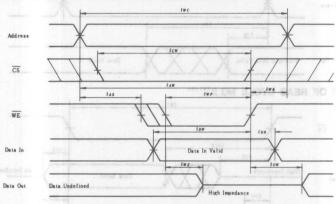
 - 6. Addresses valid prior to or coincident with $\overline{\text{CS}}$ transition low.
 - 7. This parameter is sampled and not 100% tested.



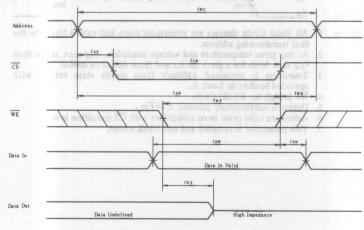
• WRITE CYCLE

Parameter	Combal	HM6147H/P-35		HM6147H/P-45		HM6147H/P-55		Unit	Notes
no Parameter	Symbol	min	max	min lo	max	min	max	Unit	Notes
Write Cycle Time	twc	35	AANO -	45	-	55		ns	(2)
Chip Selection to End of Write	tcw	35		45	1007	45	-	ns	THE RESERVE
Address Valid to End of Write	t _{AW}	35	90	45	-	45	1000	ns	The said
Address Setup Time	tas	0	-	0	DK*	0	-	ns	The Series
Write Pulse Width	twp	20	-	25	+	30		ns	4 4
Write Recovery Time	twn	0	-	0	11-1-	0		ns	25
Data Valid to End of Write	t _{DW}	20	-	25	1	25	-	ns	2.00 000
Data Hold Time	t _{DH}	10	-	10	1	10		ns	1 1952 April 1
Write Enabled to Output in High Z	twz	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	tow	0	_ (4)	0	Lio You	0	MAGHAN	ns	(3), (4)

TIMING WAVEFORM OF WRITE CYCLE (WE CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)



Note) CS or WE are High for Address Transition

Notes: 1. If CS goes high simultaneously with WE high, the output remains in a high impedance states.

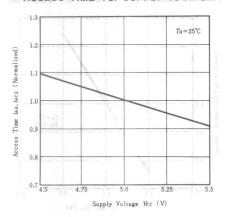
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

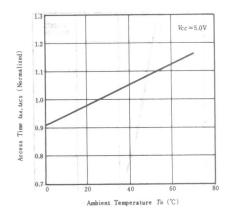
4. This parameter is sampled and not 100% tested.



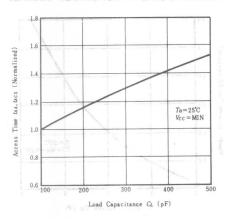
ACCESS TIME VS. SUPPLY VOLTAGE



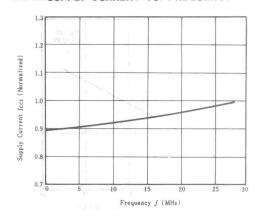
ACCESS TIME VS. AMBIENT TEMPERATURE



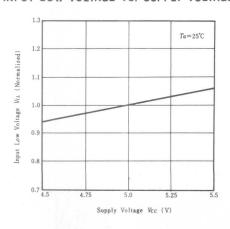
ACCESS TIME VS. LOAD CAPACITANCE



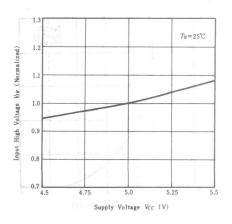
SUPPLY CURRENT VS. FREQUENCY



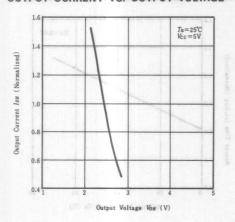
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



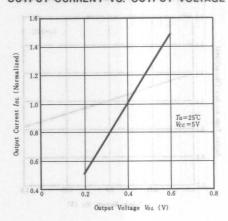
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



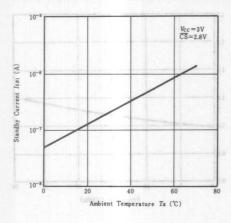
OUTPUT CURRENT VS. OUTPUT VOLTAGE



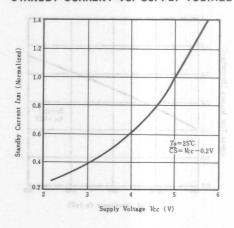
OUTPUT CURRENT VS. OUTPUT VOLTAGE



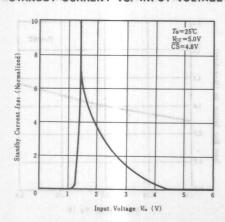
STANDBY CURRENT VS. AMBIENT TEMPERATURE



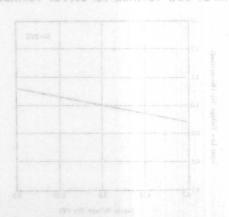
STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE



DRUT LOW VOLTAGE VS. SHEELY VOLTAGE



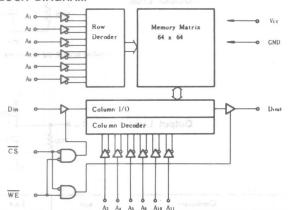
HM6147HLP-35, HM6147HLP-45, HM6147HLP-55

4096-word×1-bit High Speed Static CMOS RAM

FEATURES

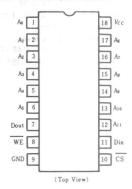
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns /55ns Max.
- Low Power Standby and Low Power Operation, Standby; 5μW typ., Operation: 150mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capable of Battery Back up Operation

BLOCK DIAGRAM



(DP-18)

PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin relative to GND	V _T	-3.5 * to +7.0	v	
DC Output Current	I_o	20	mA	
Power Dissipation	P_T	1.0	W	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature (under bias)	Tstg (bias)	-10 to +85	°C	
Storage Temperature	T_{st_g}	-55 to +125	°C	

^{*} Pulse Width 20ns. DC: -0.5V

TRECOMMENDED DC OPERATING CONDITIONS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
(i), (i) Xi an	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0.0	0	0 -	v i V
Input High (logic 1) Voltage	V_{tH}	2.2	3.0	6.0	V
Input Low (logic 0) Voltage	VIL	-0.5*	_	0.8	V

^{*} $V_{IL} \min = -3V$ (Pulse width ≤ 20 ns)

DC AND OPERATING CHARACTERISTICS (0°C $\leq Ta \leq 70$ °C, $V_{cc} = 5V \pm 10\%$, GND=0V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5$ V, GND to V_{cc}		-	10	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{out} = 0 \text{V} \sim V_{CC}$		-	10	μА
Operating Power Supply Current(1) DC	Icc	$\overline{\mathrm{CS}} = V_{IL}$, Output open	unstl_ng:	30	80	mA
Operating Power Supply Current(2) DC	Iccı	$\overline{\text{CS}} = V_{IL}$, Minimum Cycle	C SHITH I A	40	80	mA
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS} = V_{IH}$, $V_{CC} = Min$ to Max	annito's	5	15	mA
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V},$ $V_{lN} \le 0.2\text{V or } V_{lN} \ge V_{cc} - 0.2\text{V}$	- <u>V</u> tor	neM pos	100	μA
Output Low Voltage	Vol	I _{OL} = 8mA	3067	150 TU-	0.40	v
Output High Voltage	V _{OH}	$I_{OH} = -4.0 \text{mA}$	2.4	BW 214	10-9 <u>0</u> 06	V

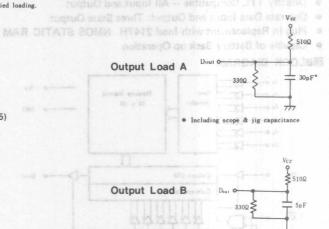
Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. Typical limits are at $V_{cc}=5.0$ V, Ta=25°C and specified loading.

MAC TEST CONDITIONS

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels:

1.5V (HM6147HLP-35) 0.8 to 2.0V (HM6147HLP-45/55)



ECAPACITANCE ($Ta=25^{\circ}C$, f=1.0 MHz)

Item	Symbol	Conditions	max	Unit
Input Capacitance	Cin	Vin=0V	5	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}$	6	pF

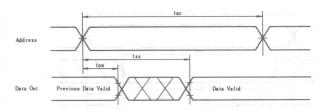
Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (Ta=0°C to 70°C, $Vcc=5V\pm10\%$, unless otherwise noted.)

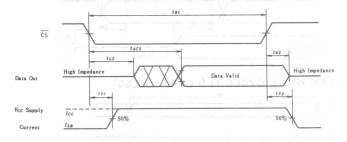
• READ CYCLE

D.	C. L.I	HM6147	HLP-35	HM6147	7HLP-45	HM6147HLP-55		Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Read Cycle Time	t _{RC}	35	14 v 1 8a-	45	-T-	55	- 03	ns	(1)
Address Access Time	tAA	-	35	-	45	-	55	ns	Dis W salas
Chip Select Access Time	tacs	5 TH 570	35	on t ake	45	ARHO	55	ns	VOD3-I
Output Hold from Address Change	toн	5	-1	5	-	5	No. 1075 a Tab	ns	
Chip Selection to Output in Low Z	tLZ	5	-	5	-	5	-	ns	(2), (3), (7)
Chip Deselection to Output in High Z	tHZ	0	30	(10)	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	tpu	0	-1	0	-	0	gental (t	ns	dgill from
Chip Deselection to Power Down Time	tpD	08.0	20	- -	20	_	20	ns	wed have

● TIMING WAVEFORM OF READ CYCLE NO.1(4)(5)(17/10/00 END BLOYS BEING



TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)



Notes: 1. All Read Cycle timings are referenced from last valid address to the first transitionining address.

2. At any given temperature and voltage condition, t_{HZ} max. is less than tLZ min. both for a given device and from device to divice.
Transition is measured ±500mV from steady state voltage with specified loading in Load B.
WE is high for READ Cycle.

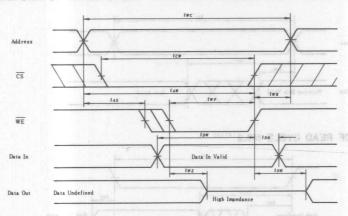
5. Device is continuously selected, \(\overline{\colong} S = V_{IL}\).
6. Addresses valid prior to or coincident with \(\overline{\colong} S\) transition low.

7. This parameter is sampled and not 100% tested.

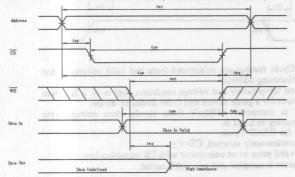
WRITE CYCLE

all band in and a within		HM6147	HLP-35	HM6147	HLP-45	HM6147HLP-55		Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Write Cycle Time	twc	35	1 4011	45	AN ACLU	55	_	ns	[2]
Chip Selection to End of Write	t cw	35	D Jagl	45	122	45	_	ns	
Address Valid to End of Write	taw	35	V (0	45	- 1	45	_	ns	
Address Setup Time	tas	0	0 AZ 0-1-	0		0	_	ns	
Write Pulse Width	twp	20	44-1-4	25	-	30	_	ns	
Write Recovery Time	t _{WR}	0	WA 36 MA	0	_	0	_	ns	
Data Valid to End of Write	t _{DW}	20	W mollows	25	4_1	25	_	ns	
Data Hold Time	t DH	10	_	10	-	10	_	ns	1
Write Enable to Output in High Z	twz	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	t ow	0	_	0	TO THE	0	_	ns	(3), (4)

● TIMING WAVEFORM OF WRITE CYCLE (WE CONTROLLED) 3.50YO GASH 3C MAD 3.50YAW CHAMIT ®



TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)



Notes: 1. If \overline{CS} goes high simultaneously with WE high, the output remains in a high impedance states.

2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

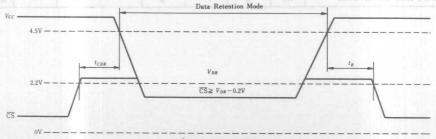
- 4. This parameter is sampled and not 100% tested.

■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

		(B) (1) (C) (1) (N)	-	_	910100 9	ENDO INCLE
Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{cc} - 0.2V$ $V_{IN} \ge V_{cc} - 0.2V \text{ or } V_{IN} \le 0.2V$	2.0	astr <u>W</u>	tid to En	Address M
Data Retention Current	ICCDR	$V_{cc} = 3.0 \text{V}, \overline{\text{CS}} \ge 2.8 \text{V}$ $V_{IN} \ge 2.8 \text{V} \text{ or } V_{IN} \le 0.2 \text{V}$	-	_	50	μA
Chip Deselect to Data Retention Time	tcDR	See Retention Waveform	0	33 -7	7 to lunch ad	ns ns
Operation Recovery Time	t _R	See Retention waveform	t RC*	-	- 000	ns

^{*} tac - Read Cycle Time.

● LOW Vcc DATA RETENTION WAVEFORM



HM6116-2, HM6116-3, HM6116-4 HM6116P-2,HM6116P-3,HM6116P-4

2048-word×8-bit High Speed Static CMOS RAM

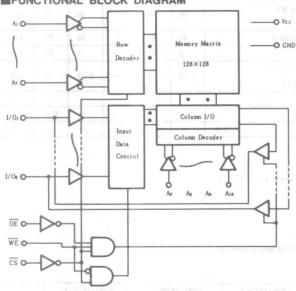
FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time

120ns/150ns/200ns (max.)

- Low Power Standby and
 Vo = 0.00 Standby: 100μW (typ.) Low Power Operation
 - Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



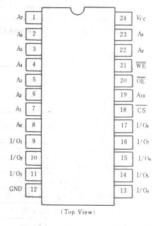
MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V_{τ}	-0.5* to +7.0	V	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature (Plastic)	Tate di	-55 to +125	°C	
Storage Temperature (Ceramic)	Tota	-65 to +150	°C	
Temperature Under Bias	Toins	-10 to +85	°C	
Power Dissipation	P_{T}	1.0	W	

^{*} Pulse Width 50ns: -1.5 V

HM6116-2, HM6116-3, HM6116-4 (DG-24) HM6116P-2, HM6116P-3, HM6116P-4 (DP-24)

PIN ARRANGEMENT



TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	I _{SB} , I _{SB1}	High Z	
L	L	Н	Read	I_{cc}	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0.00	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	VIL	-1.0*	_	0.8	V

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

■DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, GND=0V, Ta=0 to +70°C)

	0 11	17477 WINUSE 180	Н	M6116/P	-2	HM	6116/P-3	3/-4	TO.
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc}=5.5$ V, $V_{in}=$ GND to V_{cc}	1005	FRE Kur	10	Home or or	Commence	10	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I/O} = \text{GND to } V_{CC}$	-	-	10	elarC	th mis—age	10	μА
D 0 1	Icc	$\overline{\text{CS}} = V_{IL}, I_{LO} = 0 \text{mA}$	-	40	80	- AM	35	70	mA
Operating Power Supply Current Icc1**	$V_{IH} = 3.5 \text{V}, V_{IL} = 0.6 \text{V},$ $I_{L/O} = 0 \text{mA}$		35	F	=1	30		mA	
Average Operating Current	Iccz	Min. cycle, duty=100%	-	40	80	11-	35	70	mA
C. II D. C. I	I_{SB}	$\overline{\mathrm{CS}} = V_{IH}$	-	5	15	mhozař (5	15	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{is} \ge V_{cc}$ -0.2V or $V_{is} \le 0.2 \text{V}$	-	0.02	2	-	0.02	2	mA
CARRIE LA SERVICIO	17	$I_{OL} = 4 \text{mA}$	-	-	0.4	TI.		-	V
Output Voltage	Vol	I _{0L} =2.1mA	-01	asel gil	[7]	-		0.4	V
	VoH	$I_{OH} = -1.0 \text{mA}$	2.4			2.4	+	-	V

^{*} Vcc-5V, Ta-25°C

EAC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item	Symbol	HM61	116/P-2	HM6116/P-3		HM6116/P-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	t _{RC}	120	-	150		200	-	ns
Address Access Time	taa	V 1 8	120	Local	150		200	ns
Chip Select Access Time	tacs	y Te	120	-	150	-	200	ns
Chip Selection to Output in Low Z	tclz	10	+ 67 35-	15	-	15	ria in Franco	ns
Output Enable to Output Valid	toE	or + 66	80		100	(Sinss ie , I)	120	ns
Output Enable to Output in Low Z	toLZ	10	F-01-4(-	15	-	15	nolv ill so	ns
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	toHZ	0	40	0	50	0	60	ns
Output Hold from Address Change	t _{OH}	10	-	15	-	15	100.00	ns

^{**} Reference Only

• WRITE CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		***
		min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	_	150		200	_	ns
Chip Selection to End of Write	tcw	70	_	90	_	120	_	ns
Address Valid to End of Write	tAW	105		120		140	-	ns
Address Set Up Time	tas	20	_	20	-	20	-	ns
Write Pulse Width	twp	70		90	_	120	_	ns
Write Recovery Time	t w _R	5		10		10	_	ns
Output Disable to Output in High Z	t on z	0	40	/ /0	50	0	60	ns
Write to Output in High Z	t _{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t _{DW}	35		40.		60	_	ns
Data Hold from Write Time	t DH	5	70	10	-	10	_	ns
Output Active from End of Write	tow	5	_	10		10	_	ns

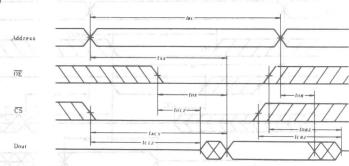
ECAPACITANCE $(f=1MHz, Ta=25^{\circ}C)$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	Cvo	$V_{l,0} = 0 \text{ V}$	5	7	pF

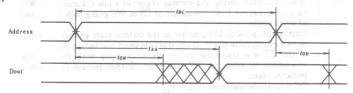
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

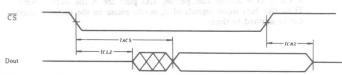
• READ CYCLE (1)(1)



● READ CYCLE (2) (1)(2)(4)

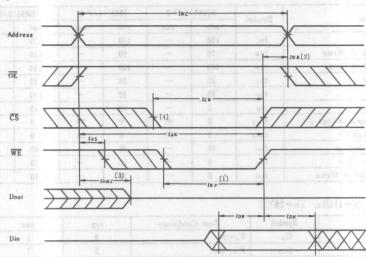


• READ CYCLE (3) (1)(3)(4)

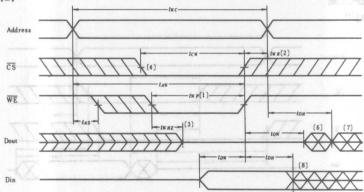


NOTES: 1. WE is High for Read Cycle.
2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low.
4. $\overline{\text{OE}} = V_{IL}$.

WRITE CYCLE (1)



• WRITE CYCLE (2) (5)

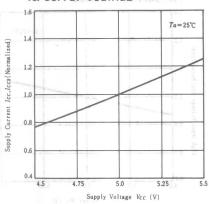


- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .

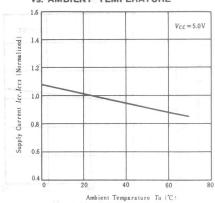
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

 - 5. OE is continuously low. $(\overline{OE} = V_{IL})$ 6. Dout is the same phase of write data of this write cycle.
 7. Dout is the read data of next address.
 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

SUPPLY CURRENT TURNE NOTE vs. SUPPLY VOLTAGE

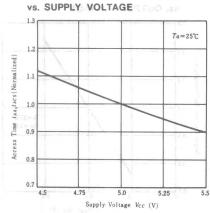


SUPPLY CURRENT vs. AMBIENT TEMPERATURE



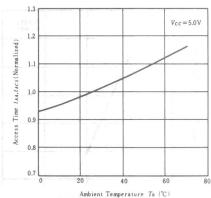
ACCESS TIME



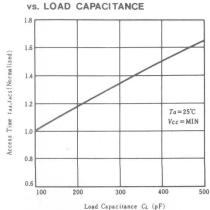


ACCESS TIME

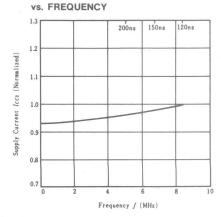
vs. AMBIENT TEMPERATURE



ACCESS TIME

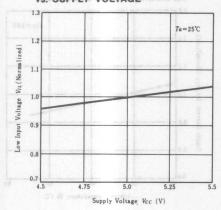


SUPPLY CURRENT

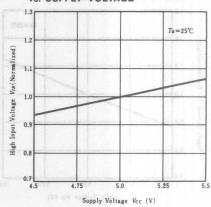


LOW INPUT VOLTAGE

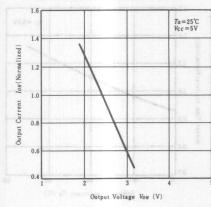
vs. SUPPLY VOLTAGE



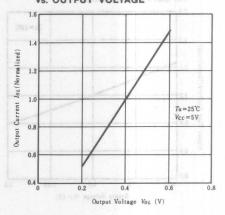
HIGH INPUT VOLTAGE

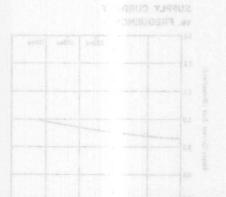


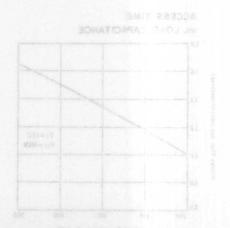
OUTPUT CURRENT
vs. OUTPUT VOLTAGE



OUTPUT CURRENT
vs. OUTPUT VOLTAGE









HM61161-2, HM61161-3, HM6116I-4

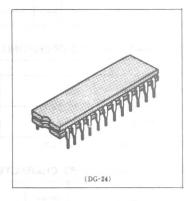
---Wide Operating Temperature Range-

2048-word×8-bit High Speed Static CMOS RAM

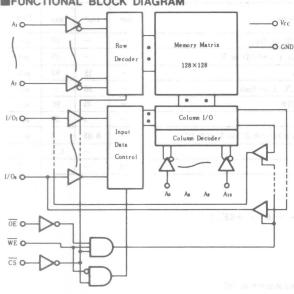
FEATURES

- Wide Operating Temperature Range −40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time
 120ns/150ns/200ns (max.)

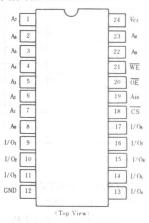
- Low Power Standby and Low Power Operation Operation: 180mW (typ.)
 - Standby: 100µW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time



FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



■ABSOLUTE MAXIMUM RATINGS

Item 81 10 Mar	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V	
Operating Temperature	T_{opr}	- 40 to +85	°C	
Storage Temperature	Tets	-65 to +150	°C	
Power Dissipation	P_T	1.0	W	

^{*} Pulse Width 50ns: -1.5 V

TRUTH TABLE TO SERVICE OF THE TRUTH TABLE OF THE TR

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	I _{SB} , I _{SB1}	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=-40 to +85°C) = 0 deliber viago2 VE signi2 =

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
	V_{IH}	2.2	3.5	6.0	V
Input Voltage	VILOR	-1.0*	NAT trabuers	0.8	V

^{*} Pulse Width: 50ns, DC: V12 min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V\pm10\%$, GND=0V, $T_a=-40$ to $+85^{\circ}$ C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	I _{LI}	V_{cc} =5.5V, V_{in} =GND to V_{cc}	-	-	10	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH}, V_{I:O} = \text{GND to } V_{CC}$	1967796	_	10	μΑ
Operating Power Supply	Icc	$\overline{\mathrm{CS}} = V_{IL}, I_{IO} = 0 \mathrm{mA}$	-	35	90	mA
Current	Icc1 **	$V_{IH} = 3.5 \text{V}, V_{IL} = 0.6 \text{V}, I_{LO} = 0 \text{mA}$	-	30	4-	mA
Average Operating Current	Iccz	Min. cycle, duty=100%	programme on a	35	90	mA
Standby Power Supply	IsB	$\overline{\text{CS}} = V_{IH}$	-	4	20	mA
Current	IsBi	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{in} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{in} \le 0.2 \text{V}$	Page!	0.02	2	mA
Output Voltage	Vol	IoL = 2.1mA	Jacob J.	-	0.4	V
Output Voitage	V _{OH}	$I_{OH} = -1.0 \text{mA}$	2.4	-	4	V

^{*} Vcc -5V, Ta-25°C

EAC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=-40$ to +85°C)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

	6 11	HM6116I-2		HM6116I-3		HM6116 I-4		11
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	tRC	120	BH <u>~ 0</u> 0)	150	- The	200	eroto s gines	ns
Address Access Time	taa	2-1	120	-	150		200	ns
Chip Select Access Time	tacs		120	1	150		200	ns
Chip Selection to Output in Low Z	tclz	10	-	10	-	10	-	ns
Output Enable to Output Valid	toE	_	80	-	100		120	ns
Output Enable to Output in Low Z	toLZ	10	-	10	_	10		ns
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	toHZ	0	40	0	50	0	60	ns
Output Hold from Address Change	t _{OH}	10		10	_	10	-	ns

^{**} Reference Only

Y	0 1 1	HM611	6 I-2	HM6116 I - 3		HM6116 I-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	t wc	120		150		200	_	ns
Chip Selection to End of Write	tcw	70	_	90	_	120	_	ns
Address Valid to End of Write	t _{AW}	105	-	120	-	140	_	ns
Address Set Up Time	tas	20	_	20	_	20	-	ns
Write Pulse Width	twp	70	- /	90		120	_	ns
Write Recovery Time	t _{WR}	5	-7.	10		10	_	ns
Output Disable to Output in High Z	toHZ	0	40	0	50	0	60	ns
Write to Output in High Z	twHZ	0	50	0	60	0	60	ns
Data to Write Time Overlap	t _{DW}	35	4/	40	_	60	_	ns
Data Hold from Write Time	t _{DH}	5	-	10		10	_	ns
Output Active from End of Write	tow	5		10	4-4-	10	_	ns

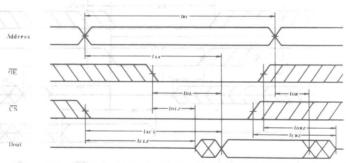
ECAPACITANCE $(f=1\text{MHz}, Ta=25^{\circ}\text{C})$

Item A	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	$C_{l imes 0}$	$V_{L/0} = 0 \text{ V}$	5	7	pF

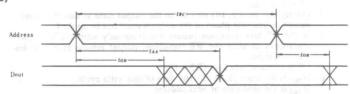
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

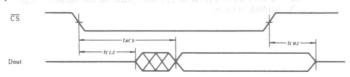
• READ CYCLE (1) (1) (5)



● READ CYCLE (2) (1) (2) (4)

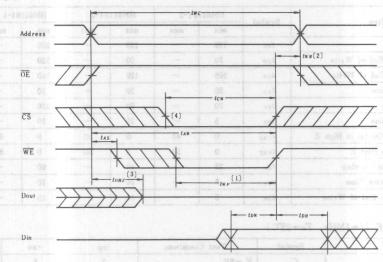


• READ CYCLE (3) (1)(3)(4)

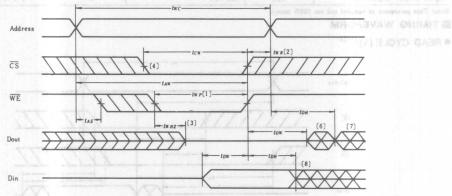


NOTES: 1. WE is High for Read Cycle.
2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low.
4. $\overline{\text{OE}} = V_{IL}$.

WRITE CYCLE (1)



• WRITE CYCLE (2) (5)



- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.

 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

 - 5. OE is continuously low. (OE = V_{IL})
 6. D_{out} is the same phase of write data of this write cycle.

 - 7. Dout is the read data of next address.
 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6116PI-2, HM6116PI-3, HM6116PI-4 — Wide Operating Ten

-Wide Operating Temperature Range-

2048-word×8-bit High Speed Static CMOS RAM

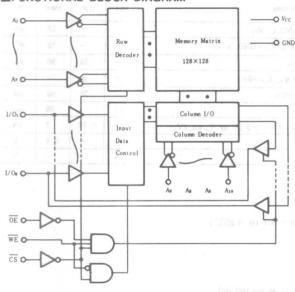
FEATURES

- Wide Operating Temperature Range −40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time

120ns/150ns/200ns (max.)

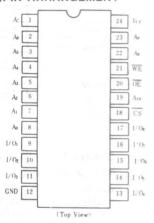
- Low Power Standby and Low Power Operation
- Standby: 100 μ W (typ.) Operation: 180mW (typ.)
- Completely Static RAM:
- No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



(DP-24)

PIN ARRANGEMENT



MABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
V_T	-0.5* to $+7.0$	V
Topr	-40 to +85	°C
Tets	-55 to +125	°C
P_T	0\$7 1.0	W
	V _T	V_{7} -0.5° to +7.0 T_{opr} -40 to +85 T_{sig} -55 to +125

^{*} Pulse Width 50ns: -1.5V

TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	I_{SB} , I_{SB1}	High Z	I I I I I I I I I I I I I I I I I I I
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

POPONIE - TORONON

a Pic Out Con pant to with Standard 19N EPN

■RECOMMENDED DC OPERATING CONDITIONS (Ta=-40 to +85°C)

Item	Symbol	Star Omin and S	typ	max	Unit
Supply Voltage	Vcc Vcc	4.5	5.0	bas 5.5	SWC RV
	GND	per Oilon: 18	0	nei 0 oO	Lo.VPewer
VV	V_{IH}	2.2	3.5	MA 6.0	descript at
Input Voltage	V_{IL}	-1.0*	ne Jugal IIA	0.8	V

^{*} Pulse Width: 50ns. DC: Vit min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, GND=0V, $T_a = -40$ to $+85^{\circ}$ C)

Item (G)	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	V_{cc} =5.5V, V_{in} =GND to V_{cc}	-		10	μА
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH}, V_{I/O} = \text{GND to } V_{CC}$	40.15	- /	10	μА
Operating Power Supply	Icc	$\overline{\text{CS}} = V_{IL}, I_{LO} = 0 \text{mA}$	-	35	90	mA
Current	Icc1 **	$V_{IH} = 3.5 \text{V}, V_{IL} = 0.6 \text{V}, I_{I/O} = 0 \text{mA}$	-	30		mA
Average Operating Current	Iccz	Min. cycle, duty=100%	1=	35	90	mA
Standby Power Supply	IsB	$\overline{\text{CS}} = V_{IH}$	-	4	20	mA
Current	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{in} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{in} \le 0.2 \text{V}$	711986	0.02	2	mA
Output Voltage	Vol	I _{0L} = 2.1mA	g/1 =/1	+1	0.4	V
Output voltage	VoH	$I_{OH} = -1.0 \text{mA}$	2.4	-		V

^{*} Vcc-5V, Ta-25°C

EAC CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = -40$ to $+85^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

Item	Symbol	HM61	HM6116PI-2		HM6116PI-3		HM6116PI-4	
1000	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	tRC	120	-55 To +12	150	+	200		ns
Address Access Time	tAA	W - 0	120	-	150	_	200	ns
Chip Select Access Time	tacs	_	120	-	150	-10	200	ns
Chip Selection to Output in Low Z	tcLż	10	-	10	-	10	_	ns
Output Enable to Output Valid	toE	-	80	_	100	_	120	ns
Output Enable to Output in Low Z	toLZ	10	-	10	-	10	_	ns
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Output Hold from Address Change	ton	10		10	_	10	_	ns

^{**} Reference Only

T.	C	HM6	116PI-2	- HM61	16PI-3	HM6116PI-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	_	150	*-	200	_	ns
Chip Selection to End of Write	tcw	70	_	90	_	120	_	ns
Address Valid to End of Write	taw	105		120		140	_	ns
Address Set Up Time	tas	20	_	20	7-1	20	_	ns
Write Pulse Width	t wp	70	_	90	-	120	_	ns
Write Recovery Time	t w _R	5		10	2 · · · · ·	10	_	ns
Output Disable to Output in High Z	toHz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	t _{DW}	35	170	40		60	_	ns
Data Hold from Write Time	t _{DH}	5	3-1	10		10	_	ns
Output Active from End of Write	tow	5	-	10	-	10	_	ns

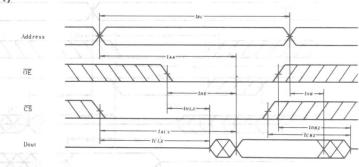
ECAPACITANCE $(f=1MHz, Ta=25^{\circ}C)$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	$C_{\nu o}$	$V_{t > 0} = 0 \text{ V}$	5	7	pF

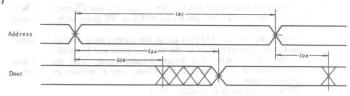
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

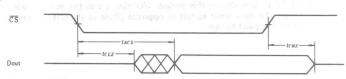
• READ CYCLE (1)(1)



■ READ CYCLE (2) (1)(2)(4)

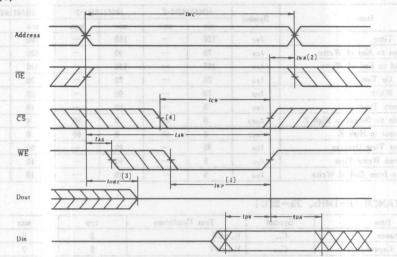


• READ CYCLE (3) (1)(3)(4)

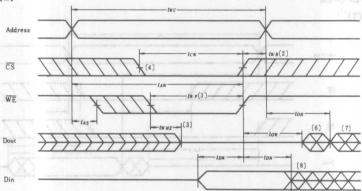


NOTES: 1. WE is High for Read Cycle.
2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low.
4. $\overline{\text{OE}} = V_{IL}$.

WRITE CYCLE (1)



• WRITE CYCLE (2) (5)



- NOTES: 1. A write occurs during the overlap $(t_{\overline{WP}})$ of a low \overline{CS} and a low \overline{WE} .

 2. $t_{\overline{WR}}$ is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

 - 5. OE is continuously low. (OE = V_{IL})
 6. D_{out} is the same phase of write data of this write cycle.

 - Dout is the read data of next address.

 If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

(C) BLOWD GARRS

HM6116FP-2, HM6116F HM6116FP-4

2048-word×8-bit High Speed Static CMOS RAM

FEATURES

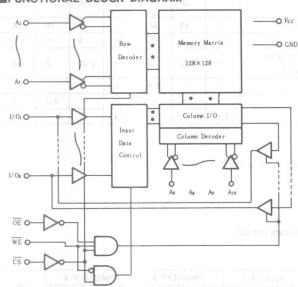
- High Density Small-Sized Package
- Projection Area Reducced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time

120ns/150ns/200ns (max.)

- Low Power Standby
- Standby:
- 100μW (typ.)

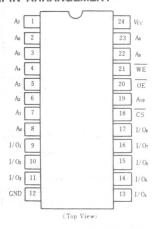
- Low Power Operation;
- Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required • Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



(FP-24)

PIN ARRANGEMENT



MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C
Temperature Under Bias	Thins	-10 to +85	°C
Power Dissipation	P_T	1.0	W

TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	I_{SB} , I_{SB1}	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle(1)~(3
L	Н	L	Write	Icc	Din	Write Cycle(1)
L	L	L	Write	Icc	Din	Write Cycle(2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	00000	0 0 8	X b To V-84-0
	V_{IH}	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	- 1	0.8	V

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

■DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, GND=0V, Ta=0 to +70°C)

	0 1 1	T . G . W.	Н	M6116FF	-2	Н	M6116FP	-3/-4	Sing
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	I _{LI}	V_{cc} =5.5V, V_{in} =GND to V_{cc}	AGDUE'	-	10	- 1	0.011118	10	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH}$ $V_{I \sim 0} = \text{GND to } V_{CC}$	mi Ero osuO l	n sip o lo	10	(NA)	Smitch Smitch	10	μА
Operating Power Supply Current	Icc	$\overline{\mathrm{CS}} = V_{IL}, I_{L'0} = 0 \mathrm{mA}$	_	40	80	Tolor	35	70	mA
	Icc1**	$V_{lH} = 3.5 \text{V}, V_{lL} = 0.6 \text{V},$ $I_{LO} = 0 \text{mA}$	_	35	ASDA	0 20	30	NOTT	mA
Average Operating Current	Iccz	Min. cycle, duty=100%	_	40	80		35	70	mA
	IsB	$\overline{\text{CS}} = V_{IH}$	X111.0	5	15	2600	5	15	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{is} \ge V_{cc}$ -0.2V or $V_{is} \le 0.2 \text{V}$	- 1	0.02	2	Decade	0.02	2	mA
A 15	77	$I_{OL} = 4 \text{mA}$	_	-	0.4		- 2	-	V
Output Voltage	Vol	$I_{OL}=2.1\text{mA}$	1 *	*+	many ye	-		0.4	V
	Von	$I_{OH} = -1.0 \text{mA}$	2.4	and a	1 4	2.4			- V

^{*} Vcc=5V, Ta=25°C

EAC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100pF$ (including scope and jig)

Ta	C	HM611	6FP-2	HM6	116FP-3	HM6116FP-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	tRC	120		150	To To	200	-	ns
Address Access Time	tAA	07 0	120		150	_	200	ns
Chip Select Access Time	tacs		120	-	150		200	ns
Chip Selection to Output in Low Z	tclz	10	-	15		15	111.0.1-100001	ns
Output Enable to Output Valid	toE		80		100	_	120	ns
Output Enable to Output in Low Z	toLz	10		15	1	15	15terJ &	ns
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t _{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t on	10		15	-	15		ns

^{**} Reference Only

T-	0 1 1	HM61	16FP-2	HM611	16FP-3	HM611	6FP-4	I I - 24
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	t wc	120	_	150	7	200	_	ns
Chip Selection to End of Write	tcw	70		90		120	_	ns
Address Valid to End of Write	tAW	105	_	120		140	_	ns
Address Set Up Time	tas	20	_	20	+/	20	_	ns
Write Pulse Width	twp	70	_	90	_	120	_	ns
Write Recovery Time	tw _R	5	- /	10		10	_	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	twHZ	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	-/ 7	40		60	_	ns
Data Hold from Write Time	t _{DH}	5		10	-	10	_	ns
Output Active from End of Write	tow	- 5	_	10		10	_	ns

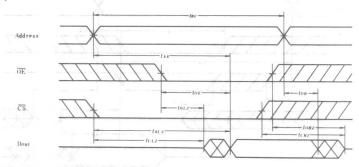
EXAMPLE 1.1 CAPACITANCE $(f=1 \text{MHz}, Ta=25^{\circ}\text{C})$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance $C_{in} = 0$ V		$V_{in} = 0V$	3	5	pF
Input/Output Capacitance	C1/0	$V_{I\nearrow0}=0\mathrm{V}$	5	7	pF

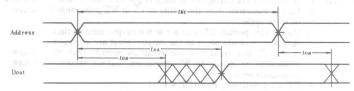
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

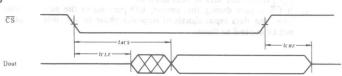
● READ CYCLE (1) (1)



● READ CYCLE (2) (1)(2)(4)



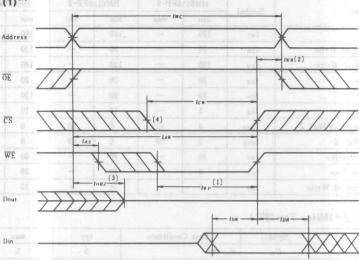
• READ CYCLE (3) (1)(3)(4)



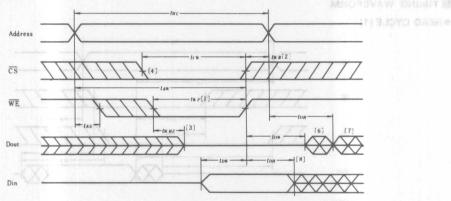
NOTES: 1. $\overline{\text{WE}}$ is High for Read Cycle. 2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$. 3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low. 4. $\overline{\text{OE}} = V_{IL}$.

TIMING WAVEFORM

• WRITE CYCLE (1) (1)



• WRITE CYCLE (2) (5)



- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.

 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

 - impedance state.

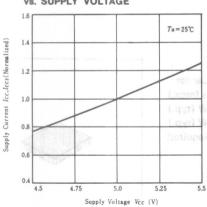
 OE is continuously low. (OE = V_{IL})

 Dout is the same phase of write data of this write cycle.

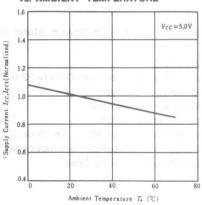
 Dout is the read data of next address.

 If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

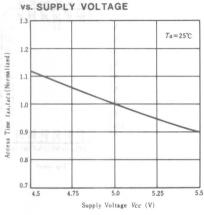
SUPPLY CURRENT
VS. SUPPLY VOLTAGE



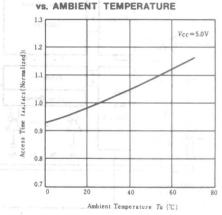
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



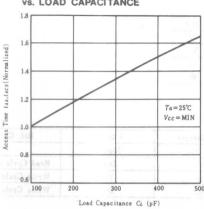
ACCESS TIME



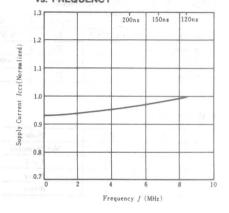
ACCESS TIME



ACCESS TIME
vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. FREQUENCY



HM6116CG-2, HM6116CG-3, HM6116CG-4

2048-word×8-bit High Speed Static CMOS RAM

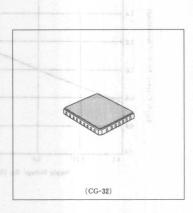
FEATURES

- Single 5V Supply and High Density 32 pin-Leadless-Chip Carrier
- High speed: Fast Access Time 120ns/150ns/200ns (max.)

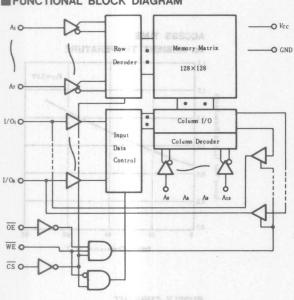
 Low Power Standby and Low Power Operation

Standby: 100µW (typ.) Operation: 180mW (typ.)

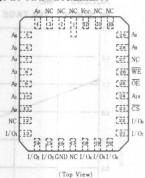
- Completely Static RAM: No Clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time



FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



MADE ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tets	-65 to +150	°C	
Power Dissipation	P_T	1.0	W	

^{*} Pulse Width 50ns: -1.5V

TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle			
Н	×	×	Not Selected	I _{SB} , I _{SB1}	High Z				
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3)			
L	Н	L	Write	Icc	Din	Write Cycle (1)			
L	L	L	Write	Icc	Din	Write Cycle (2)			

TRECOMMENDED DC OPERATING CONDITIONS $(Ta=0 \text{ to } +70^{\circ}\text{C})$

It	em		Symbol	min	typ	max	Unit
7. SET	nise	zah	Vcc Vcc	4.5	5.0	5.5	V
Supply Voltage		GND	08.0	0	0	V	
Input Voltage		V _{IH}	2.2	3.5	6.0	V	
		VIL	-1.0*		0.8	V	

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, GND=0V, Ta=0 to +70°C)

an 09 9	0	0 08 0	H	M6116CG	-2	HM	6116CG-	3/-4	Unit
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5 \text{V}$, $V_{in} = \text{GND to } V_{cc}$		10.2	10	_	_	10	μА
Output Leakage Current	I _{LO}	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{L'O} = \text{GND to } V_{CC}$	_	- ag1	10	_	_	10	μА
Operating Power Supply	Icc	$\overline{CS} = V_{IL}, I_{L/0} = 0 \text{mA}$	-	40	80	-	35	70	mA
	Icc1 **	$V_{tH} = 3.5 \text{V}, V_{tL} = 0.6 \text{V},$ $I_{t>0} = 0 \text{mA}$	t. √0=,√	35	erye y =	_	30	-	mA
Average Operating Current	Iccz	Min. cycle, duty=100%	2.7	40	80	_	35	70	mA
	I_{SB}	$\overline{\mathrm{CS}} = V_{IH}$	_	5	15	_	5	15	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{is} \ge V_{cc}$ -0.2V or $V_{is} \le 0.2 \text{V}$	_	0.02	2	_	0.02	2	mA
	**	$I_{OL} = 4 \text{mA}$	_	-	0.4	_	_	-	V
Output Voltage	Vol	$I_{OL}=2.1\text{mA}$	-	-	_	, -	_	0.4	V
	V_{OH}	$I_{OH} = -1.0 \text{mA}$	2.4		-	2.4	_	_	V

^{*} $V_{CC} = 5V$, $Ta = 25^{\circ}C$

EAC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

Item	Symbol	HM6116CG-2		HM6116CG-3		HM6116CG-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	t _{RC}	120	1	150	_	200	-	ns
Address Access Time	taa	V-V	120		150	_	200	ns
Chip Select Access Time	tacs	m	120		150	_	200	ns
Chip Selection to Output in Low Z	tclz	10	_	15	_	15	_	ns
Output Enable to Output Valid	t _{OE}	_	80	_	100	_	120	ns
Output Enable to Output in Low Z	toLz	10	_	15	- 	15	_	ns
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t _{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t _{OH}	10	VAL	15	_	15	_	ns



^{**} Reference Only

Hall yang	Combal	HM61	16CG-2	HM61	HM6116CG-3		16CG-4	Unit
Item 2.2	Symbol	min	max	min	max	min	max	Ont
Write Cycle Time	twc	120	-	150	-	200	- 191	ns
Chip Selection to End of Write	tcw	70		90	-	120		ns
Address Valid to End of Write	taw	105		120	-	140	- 93	ns
Address Set Up Time	tas	20	-	20		20	_	ns
Write Pulse Width	t wp	70	-	90	_ VI	120	94 <u>million</u>	ns
Write Recovery Time	t wR	5	_	10	_	10	_	ns
Output Disable to Output in High Z	toHZ	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	t _{DW}	35	91/0/11/01	40	1001	60	_81911	ns
Data Hold from Write Time	t _{DH}	5	na riika	10	N - 1	10	- 5	ns
Output Active from End of Write	tow	5	-	10	-	10	_	ns

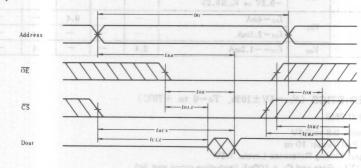
ECAPACITANCE $(f=1\text{MHz}, Ta=25^{\circ}\text{C})$

Item	Symbol	Test Conditions	typ	max kname n	Unit
Input Capacitance	Cin	Vin=0V	3	5	pF
Input/Output Capacitance	Cvo	$V_{l,\infty} = 0 \text{ V}$	5	7	pF

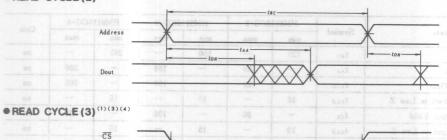
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

• READ CYCLE (1)(1)



• READ CYCLE (2) (1)(2)(4)



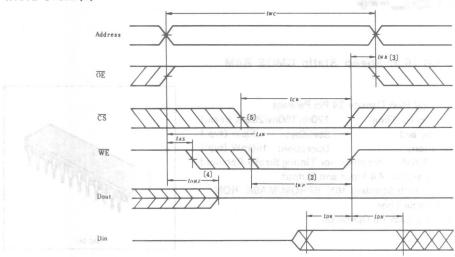
NOTES: 1. WE is High for Read Cycle.

Device is continuously selected, S = V_{IL}.
 Address Valid prior to or coincident with S transition Low.

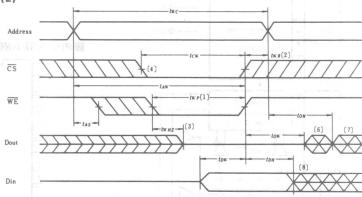
4. $\overline{OE} = V_{IL}$.

Dout

WRITE CYCLE(1)(1)



● WRITE CYCLE (2) (5)



- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.

 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.

 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the S low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

 - pedance state.
 5. OE is continuously low. (OE = V_{IL})
 6. Dout is the same phase of write data of this write cycle.
 7. Dout is the read data of next address.
 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6116L-2, HM6116L-3, HM6116L-4

2048-word×8-bit High Speed Static CMOS RAM

FEATURES

Single 5V Supply and High Density 24 Pin Package

 High Speed: Fast Access Time Low Power Standby and

120ns/150ns/200ns (max.) Standby: 20μW (typ.)

Low Power Operation:

Operation: 160mW (typ.)

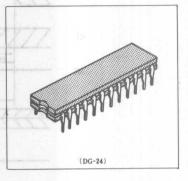
Completely Static RAM: No clock nor Timing Strobe Required

Directly TTL Compatible: All Input and Output

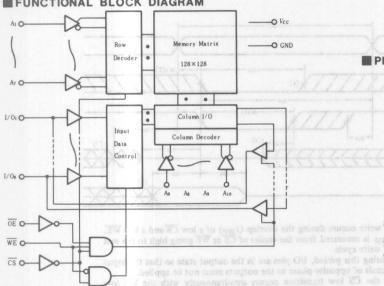
Pin Out Compatible with Standard 16K EPROM/MASK ROM

Equal Access and Cycle Time

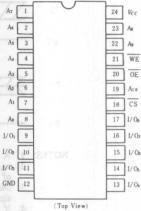
Capability of Battery Back up Operation



FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	of VT	-0.5* to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tets	-65 to +150	°C
Temperature Under Bias	Thias	-10 to +85	°C o
Power Dissipation	P_T	1.0	W

^{*} Pulse Width 50ns: -1.5V

TRUTH TABLE

CS	ŌE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, IsB1	High Z	THE SALES
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS $(Ta=0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol S-	min	typ	max	Unit
Supply Voltage	Wcc 184	4.5	5.0	5.5	V
	GND	0	0	0	V
051	VIH	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	- W. T	0.8	V

^{*} Pulse Width: 50ns, DC: V/L min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V\pm10\%$, GND=0V, $T_a=0$ to $+70^{\circ}$ C)

. 60 0	0 1 10	70 . 0 . 111	HM	16116L/F	7-2	HM6	116L/P-	3/-4	77.
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	ILI	V_{CC} =5.5V, V_{in} =GND to V_{CC}	+	V +	2	-	_	2	μA
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I \neq 0} = \text{GND to } V_{CC}$		<u> </u>	2	<u>-</u>	-	2	μΑ
O	Icc	$\overline{\text{CS}} = V_{IL}, I_{I/O} = 0 \text{mA}$	_	35	70	_	30	60	mA
Operating Power Supply Current	Icc1**	$V_{IH} = 3.5 \text{ V}, V_{IL} = 0.6 \text{ V},$ $I_{I>0} = 0 \text{ mA}$	n	30	6.415	_	25	_	mA
Average Operating Current	Icc 2	min. cycle, duty=100%	-	35	70	_	30	60	mA
C. II D. C. I	IsB	$\overline{\mathrm{CS}} = V_{IH}$	V .	4	12	_	4	12	mA
Standby Power Supply Current	Issi	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, \ V_{in} \ge V_{CC} - 0.2 \text{V}$ or $V_{in} \le 0.2 \text{V}$	_	4	100		4	100	μΑ
	**	$I_{OL} = 4 \text{mA}$	_	_	0.4	_	_	_	.,,
Output Voltage	Vol	$I_{OL}=2.1\text{mA}$	_	_	-	_	_	0.4	V
	Von	$I_{OH} = -1.0 \text{mA}$	2.4			2.4	_	_	V

^{* :} Vcc-5V, Ta-25°C

AC CHARACTERISTICS ($V_{cc}=5V \pm 10\%$, $T_a=0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100pF$ (including scope and jig)

Ta	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
Item	Symbol	m in	max	min	max	min	max	Unit
Read Cycle Time	t _{RC}	120	_	150	-	200	_	ns
Address Access Time	taa		120		150	-	200	ns
Chip Select Access Time	tacs	A - X - X	120	- 800	150	_	200	ns
Chip Selection to Output in Low Z	tcLZ	10	W-	15	_	15	_	ns
Output Enable to Output Valid	t o E	_	80	_	100	_	120	ns
Output Enable to Output in Low Z	toLZ	10	_	15	_ "	15	_	ns
Chip deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	- t онг	0	40	0	50	0	60	ns
Output Hold from Address Change	tон	10		15		15	_	ns



^{* * :} Reference Only

21aU 1.500	CL-1	HM6	116L-2	HM6116L-3		HM61	16L-4	TT-:4
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	-	150	_	200	- 6	ns
Chip Selection to End of Write	tcw	70	T 1 -	90		120	-	ns
Address Valid to End of Write	t AW	105	-	120	-	140	- 4	ns
Address Set Up Time	tas	20		20		20		ns
Write Pulse Width	twp	70	-	90	- "	120	1 20_ante	ns
Write Recovery Time	twr	5	2011	10	CATION	10	1200.0	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	t whz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	-	40	-	60	_	ns
Data Hold from Write Time	t DH	5	of ()/(0 ==	10	1 - Vest	10	install is	ns
Output Active from End of Write	tow	5	1075 14	10	25 F	10	-	ns

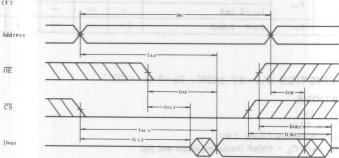
EXAMPLE 1 CAPACITANCE $(f=1\text{MHz}, Ta=25^{\circ}\text{C})$

Item	Symbol	Test Conditions typ max			Test Conditions		typ max		Unit
Input Capacitance	Cin	Vin-OV	data = 100%	3	1101	5	pF		
Input/Output Capacitance	Ciro	$V_{I \neq O} = 0 \text{ V}$		W - 5	44.	7	pF		

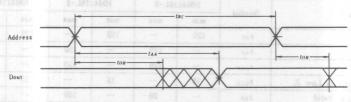
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

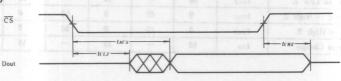
• Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)

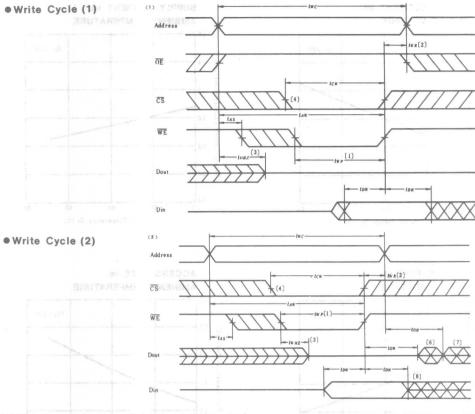


Read Cycle (3) (1), (3), (4)



NOTES: 1. WE is High for Read Cycle.

- Device is continuously selected, \$\overline{CS}\$ = \$V_{IL}\$.
 Address Valid prior to or coincident with \$\overline{CS}\$ transition Low.
- 4. $\overline{OE} = V_{IL}$.



NOTES: 1. A write occurs during the overlap (twp) of a low CS and a low WE.

- 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.

 3. During this period, I/O pins are in the output
- state so that the input signals of opposite phase to the outputs must not be applied.
- 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE

transition, output remain in a high impedance

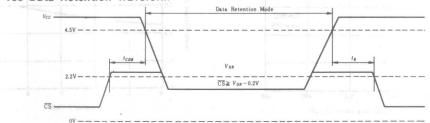
- 5. \overline{OE} is continuously low. $(\overline{OE} = V_{IL})$ 6. D_{out} is the same phase of write data of this write cycle.
- 7. D_{out} is the read data of next address.
 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

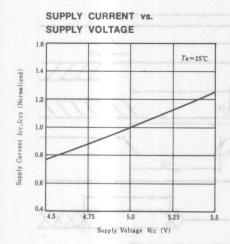
■LOW VCC DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

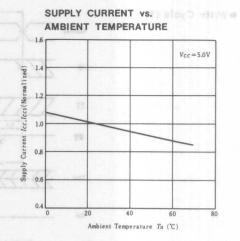
Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, \ V_{in} \ge V_{CC} - 0.2 \text{V} \text{ or } V_{in} \le 0.2 \text{V}$	2.0	_	_	V
Data Retention Current	Iccor*	$V_{CC}=3.0\text{ V}, \ \overline{\text{CS}} \ge 2.8\text{ V}, \ V_{in} \ge 2.8\text{ V} \text{ or } V_{in} \le 0.2\text{ V}$	_	_	50	μΑ
Chip Deselect to Data Retention Time	tcor	C D W	0	_	_	ns
Operation Recovery Time	t _R	See Retention Waveform	t RC **	_	_	ns

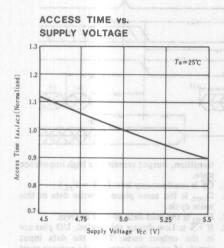
^{*} V_{IL}=-0.3V min. ** t_{RC}=Read Cycle Time.

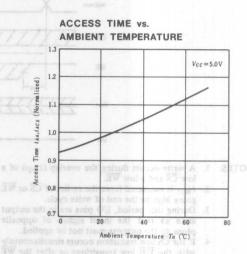
● Low Vcc Data Retention Waveform

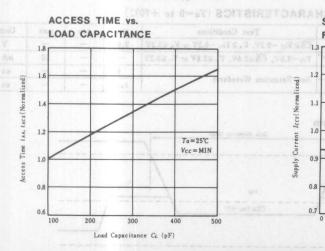


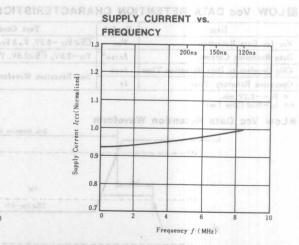












1.3

1.2

(pazi | 1.1)

1.2

(pazi | 1.1)

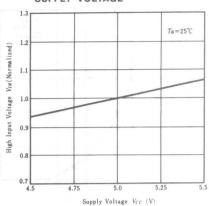
1.0

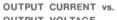
(pazi | 0.1)

1

LOW INPUT VOLTAGE vs.

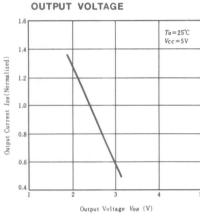
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



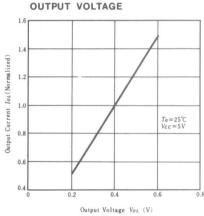


Supply Voltage V_{CC} (V)

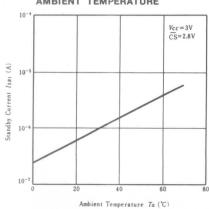
0.8



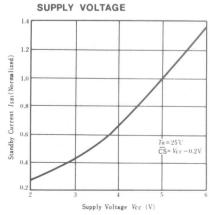
OUTPUT CURRENT vs.



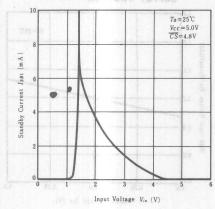
STANDBY CURRENT vs. AMBIENT TEMPERATURE



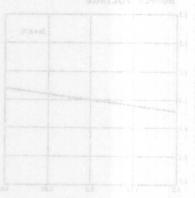
STANDBY CURRENT vs.



STANDBY CURRENT VS.



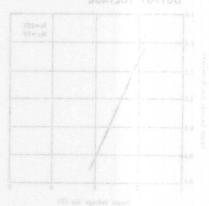
LOW HARDT VOLTAGE VS.



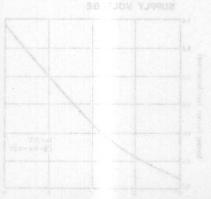
OUTPUT OUT 187 VS.



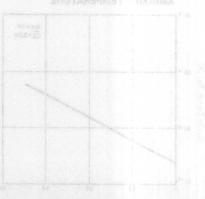
ANTENN CHRENT ANTENNA



STANDBY CL SOIT VS.



STANDER CURRENT VS.



HM6116LI-2, HM6116LI-3, HM6116LI-4

--- Wide Operating Temperature Range

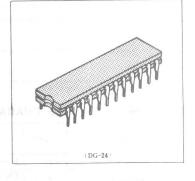
2048-word × 8-bit High Speed Static CMOS RAM

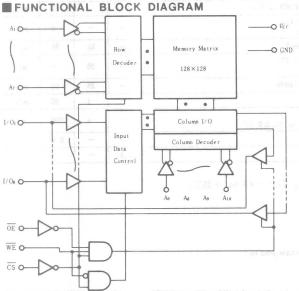
FEATURES

- Wide Operating Temperature Range −40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time

120ns/150ns/200ns (max.)

- Low Power Standby and
- 20μW (typ.) Standby:
- Low Power Operation;
- Operation: 160m W (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation



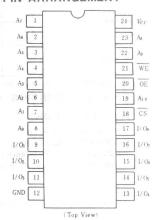


MADE ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to $+7.0$	V
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tate	-65 to +150	°C
Power Dissipation	P_T	1.0	W

^{*} Pulse Width 50ns: - 1.5 V

PIN ARRANGEMENT



TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, IsB1	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

RECOMMENDED DC OPERATING CONDITIONS $(Ta = -40 \text{ to } +85^{\circ}\text{C})$

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
	VIH	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	an stopen old	0.8	V

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V \pm 10\%$, GND=0V, $T_a=-40$ to $+85^{\circ}$ C)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input Leakage Current		$V_{cc}=5.5$ V, $V_{in}=$ GND to V_{cc}	DIAGRAM	3040.L	a - Al	2	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I \neq 0} = \text{GND to } V_{CC}$		-	1=3	2	μA
O	Icc	$\overline{\text{CS}} = V_{IL}, I_{I > 0} = 0 \text{mA}$	a Manney Marris		35	90	mA
Operating Power Supply Current	Icc1**	$V_{IH} = 3.5 \text{V}, V_{IL} = 0.6 \text{V}, I_{I \neq 0} = 0 \text{mA}$	851 X 857	rul <u>us</u> -l	30	-	mA
Average Operating Current	Icc 2	min. cycle, duty = 100%		-	35	90	mA
Caralla Danie Caral	IsB	$\overline{CS} = V_{IH}$	17 1	t	4	20	mA
Standby Power Supply Current	Isbı	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V},$ $V_{is} \ge V_{cc} - 0.2\text{V or } V_{is} \le 0.2\text{V}$	-Distance (20)	-	4	200	μΑ
0	Vol	IoL=2.1mA	Colone Decodes	hrim	-	0.4	V
Output Voltage	Von	$I_{OH} = -1.0 \text{mA}$	THE STATE OF	2.4	- 1	/ -	V

^{* :} Vcc - 5V, Ta - 25°C * * : Reference Only

\blacksquare AC CHARACTERISTICS ($V_{cc}=5V~\pm10\%$, $T_a=-40~\text{to}~+85^{\circ}\text{C}$

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

Fire Water	6 11	HM61	16LI-2	HM6116LI-3		HM6116LI-4		UCE BAS	
Item	Symbol	min	max	min	max	min	max	Unit	
Read Cycle Time	t RC	120	T + et 18.	150	V - 0	200	M ATT M	ns	
Address Access Time	taa	3" - 8	120	-	150	_	200	ns	
Chip Select Access Time	tacs	0 - 0	120		150	_	200	ns	
Chip Selection to Output in Low Z	tclz	10	1 -	10	11 -1	10	<u>do</u> 1781	ns	
Output Enable to Output Valid	toE	-	80	_	100	-	120	ns	
Output Enable to Output in Low Z	toLZ	10	-	10	-	10		ns	
Chip deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	t on	10	_	10		10	-	ns	

T.	C 1.1	HM61	16LI-2	HM61	16LI-3	HM6116LI-4		Unit	
Item	Symbol	min	max	min	max	min	max	Unit	
Write Cycle Time	twc	120	_	150	7 -	200	_	ns	
Chip Selection to End of Write	tcw	70		90	_	120	_	ns	
Address Valid to End of Write	t _{AW}	105	-	120	7-	140	_	ns	
Address Set Up Time	tas	20	===	20		20	_	ns	
Write Pulse Width	twp	70		90	_	120	_	ns	
Write Recovery Time	t w R	5	-21	10	_	10	_	ns	
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Write to Output in High Z	twnz	0	50	0	60	0	60	ns	
Data to Write Time Overlap	- t DW	35	_	40	_	60	_	ns	
Data Hold from Write Time	t DH	5	_	10	_	10	_	ns	
Output Active from End of Write	tow	5	-	10	_	10	-	ns	

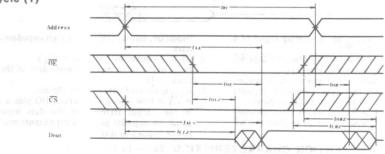
CAPACITANCE $(f=1\text{MHz}, Ta=25^{\circ}\text{C})$

Item	Symbol Test Conditions		typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	C1/0	$V_{10} = 0 \text{ V}$	5	7	pF

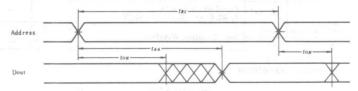
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

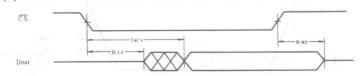
● Read Cycle (1) (1), (5)



● Read Cycle (2) (1), (2), (4)



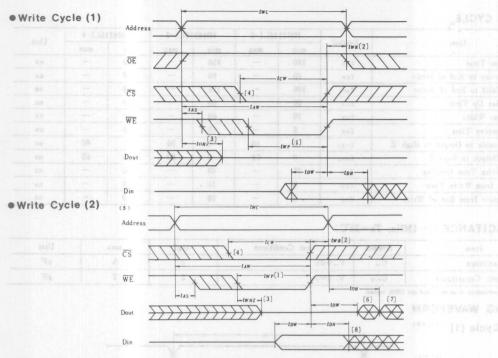
(1), (3), (4) Read Cycle (3)



NOTES: 1. WE is High for Read Cycle.

Device is continuously selected, \$\overline{CS}\$ = \$V_{IL}\$.
 Address Valid prior to or coincident with \$\overline{CS}\$ transition Low.

4. $\overline{OE} = V_{IL}$.



NOTES: 1. A write occurs during the overlap (twp) of a low CS and a low WE.

- 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
- 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE

transition, output remain in a high impedance

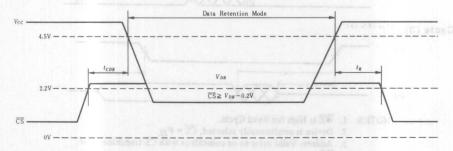
- 5. \overline{OE} is continuously low. $(\overline{OE} = V_{II})$
- 6. Dout is the same phase of write data of this write cycle.
- D_{out} is the read data of next address.
 If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW VCC DATA RETENTION CHARACTERISTICS (Ta=-40 to +85°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \ V_{is} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{is} \le 0.2 \text{V}$	2.0	-(2)	81-77-7	V
Data Retention Current	Iccor*	I_{CCDR}^* $V_{CC} = 3.0 \text{ V}, \overline{CS} \ge 2.8 \text{ V}, V_{I*} \ge 2.8 \text{ V} \text{ or } -0.3 \text{ V} \le V_{I*} \le 0.2 \text{ V}$		_	100	μA
Chip Deselect to Data Retention Time	tcor	0 0 0	0		-	ns
Operation Recovery Time	t R	See Retention Waveform	t RC **	_	_	ns

^{*} $V_{IL} = -0.3 \text{ V}$ min. ** $t_{RC} = \text{Read Cycle Time}$.

Low Vcc Data Retention Waveform



2048-word×8-bit High Speed Static CMOS RAM

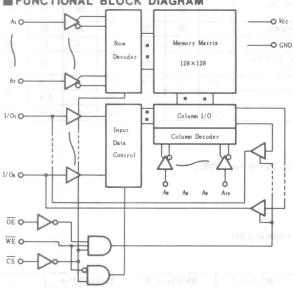
FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time

120ns/150ns/200ns (max.)

- Low Power Standby and
- Standby: $10\mu W$ (typ.)
- Low Power Operation;
- Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
 Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

FUNCTIONAL BLOCK DIAGRAM



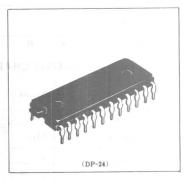
MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tate	-55 to +125	°C	
Temperature Under Bias	Thins	-10 to +85	°C.	
Power Dissipation	P_{T}	1.0	W	

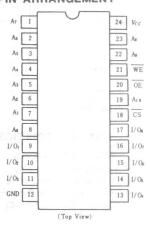
^{*} Pulse Width 50ns: -1.5V

TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, IsB1	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)



PIN ARRANGEMENT



■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
	Vcc	4.5	5.0	5.5	IOW V
Supply Voltage	GND	0	0	0	V
Input Voltage	VIH	2.2	3.5	6.0	V
	VIL	-1.0*	igh Desity 24	0.8	Va e v

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

■ DC AND OPERATING CHARACTERISTICS (Vcc=5V ±10%, GND=0V, Ta=0 to +70°C)

TANK THE RESERVE	0 1 1	ung Strobe Flaquingd	Н	M6116LP	-2	HM	6116LP-3	3/-4	O e
Item	Symbol	mbol Test Conditions		typ*	max	min	typ*	max	Unit
Input Leakage Current	Iu	$V_{cc}=5.5$ V, $V_{in}=$ GND to V_{cc}	4.45 N	DI DIS	2	ALAN DI	16 (41710)	2	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I \times O} = \text{GND to } V_{CC}$	-0.0	Us re gC	2	albyo vary Bu	ne see	2	μA
Operating Power Supply	Icc	$\overline{CS} = V_{IL}, I_{III} = 0 \text{mA}$	-	35	70	_	30	60	mA
Current	Icc1**	$V_{IB} = 3.5 \text{V}, \ V_{IL} = 0.6 \text{V}, \ I_{I > 0} = 0 \text{mA}$		30	N DIS	0038	25	HE CHA	mA
Average Operating Current	Icc 2	min. cycle, duty = 100%	-	35	70	-	30	60	mA
C. 11 D. C. 1	Isa	$\overline{CS} = V_{IH}$	<u> </u>	4	12		4	12	mA
Standby Power Supply Current	Isbi	$\overline{\text{CS}} \ge V_{CC} - 0.2\text{V}, \ V_{in} \ge V_{CC} - 0.2\text{V} \text{ or } V_{in} \le 0.2\text{V}$	- 8	× 11 2	50	Street,	2	50	μА
A III	THE WAR	IoL-4mA	_	-	0.4	-	- 30	-	0 14
Output Voltage	Vol	IoL = 2.1mA	70	-	-	12-	-	0.4	V
	Von	$I_{OH} = -1.0 \text{mA}$	2.4	oninto)	12	2.4	-1		V

^{* :} Vec-5V, Ta-25°C

AC CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

	C 1.1	HM61	16LP-2	HM6116LP-3		HM6116LP-4		I I I I I	
Item	Symbol	m in	max	min	max	min	max	Unit	
Read Cycle Time	t RC	120	gaitell	150	e 1-	200	crest/	ns	
Address Access Time	taa V	7.0-	120		150	of sylls to	200	ns	
Chip Select Access Time	tacs	-07+	120		150	-	200	ns ns	
Chip Selection to Output in Low Z	tclz	10	61 23-	15	-	15	rute a p pe	ns	
Output Enable to Output Valid	toE		80	_0013	100	-2"	120	ns	
Output Enable to Output in Low Z	toLZ	10	-	15	1	15	6401 YE (184	ns	
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	t on	10	-	15	-	15	10 - T	ns	

^{* * :} Reference Only

Y	C 1.1	HM61	16LP-2	HM61	16LP-3	HM61	16LP-4	TI-:
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	100 min (150		200	-	ns
Chip Selection to End of Write	tcw	70	_	90	- -	120	_	ns
Address Valid to End of Write	t _{AW}	105		120	_	140	_	ns
Address Set Up Time	tas	20	177	20	77	20	_	ns
Write Pulse Width	twp	70	14-1-	90	_	120	-	ns
Write Recovery Time	t w _R	5	_	10	_	10	_	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	t w H Z	0	50	0	60	0	60	ns
Data to Write Time Overlap	t DW	35		40	,	60	_	ns
Data Hold from Write Time	t DH	5		10	- T	10	-	ns
Output Active from End of Write	tow	5	_	10	_	10	_	ns

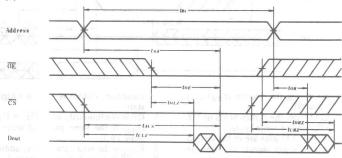
CAPACITANCE $(f=1\text{MHz}, Ta=25^{\circ}\text{C})$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	C1.0	$V_{I=0} = 0 \text{ V}$	5	7	pF

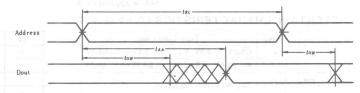
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

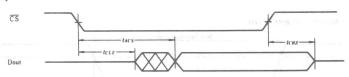
● Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)



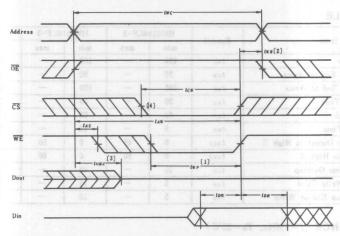
● Read Cycle (3) (1), (3), (4)



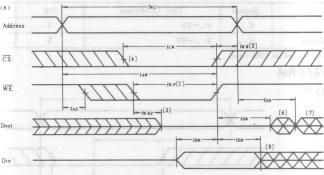
NOTES: 1. WE is High for Read Cycle.
2. Device is continuously selected, CS = V_{IL}.
3. Address Valid prior to or coincident with CS transition Low.

4. $\overline{OE} = V_{IL}$.

• Write Cycle (1)



• Write Cycle (2)



NOTES: 1. A write occurs during the overlap (twp) of a low CS and a low WE.

2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.

3. During this period, I/O pins are in the output state so that the input signals of opposite

phase to the outputs must not be applied.

4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE

transition, output remain in a high impedance

5. \overline{OE} is continuously low. $(\overline{OE} = V_{IL})$

6. Dout is the same phase of write data of this write cycle.

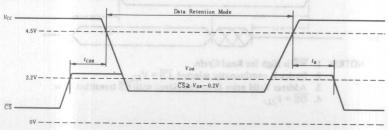
7. Dout is the read data of next address.
8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

LOW VCC DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

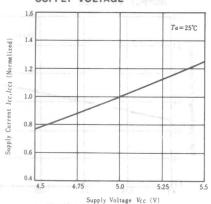
Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \ V_{in} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{in} \le 0.2 \text{V}$	2.0	_	_	V
Data Retention Current	Iccor*	$V_{cc} = 3.0 \text{ V}, \ \overline{\text{CS}} \ge 2.8 \text{ V}, \ V_{in} \ge 2.8 \text{ V} \text{ or } V_{in} \le 0.2 \text{ V}$		_	30	μΑ
Chip Deselect to Data Retention Time	tcor		0	_		ns
Operation Recovery Time	t _R	See Retention Waveform	trc**	_	_	ns

^{*} $10 \,\mu\text{A}$ max at $Ta=0\,\text{°C}$ to $+40\,\text{°C}$, V_{IL} min = $-0.3\,\text{V}$ * * $t_{RC}=\text{Read}$ Cycle Time.

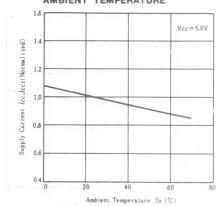
Low Vcc Data Retention Waveform



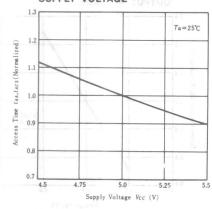
SUPPLY CURRENT vs.
SUPPLY VOLTAGE



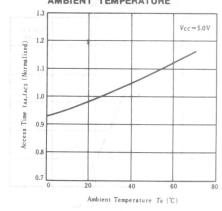
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



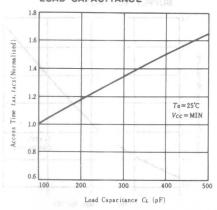
ACCESS TIME VS. TOSTUO SUPPLY VOLTAGE TUOTIO



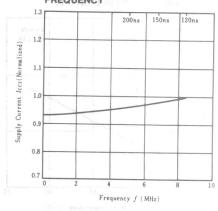
ACCESS TIME vs.
AMBIENT TEMPERATURE



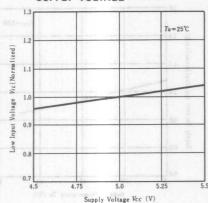
ACCESS TIME vs.
LOAD CAPACITANCE



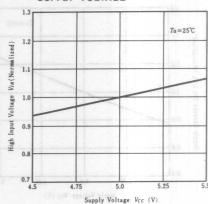
SUPPLY CURRENT vs. FREQUENCY



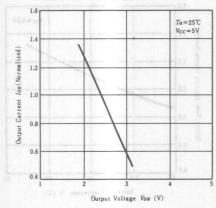
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



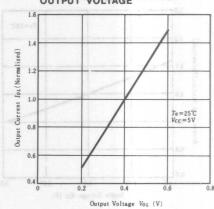
HIGH INPUT VOLTAGE VS. SUPPLY VOLTAGE



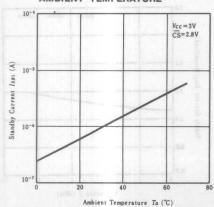
OUTPUT CURRENT vs.



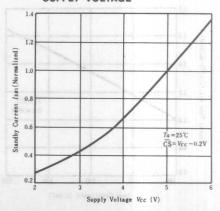
OUTPUT CURRENT vs.



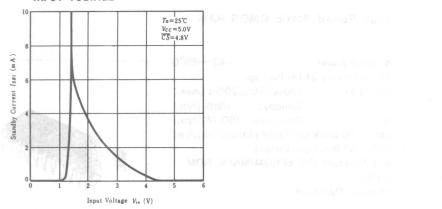
STANDBY CURRENT vs.
AMBIENT TEMPERATURE



STANDBY CURRENT vs.
SUPPLY VOLTAGE



STANDBY CURRENT vs.



HM6116LPI-2, HM6116LPI-3, HM6116LPI-4 — Wide Operating Temperature Range

2048-word×8-bit High Speed Static CMOS RAM

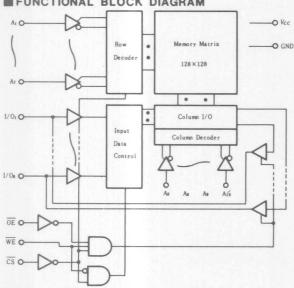
FEATURES

- -40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time

120ns/150ns/200ns (max.)

- Low Power Standby and Low Power Operation;
- Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

FUNCTIONAL BLOCK DIAGRAM

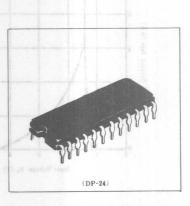


MADSOLUTE MAXIMUM RATINGS

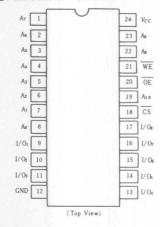
Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tate	-55 to +125	°C
Power Dissipation	P_{T}	1.0	W

^{*} Pulse Width 50ns: -1.5 V

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PIN ARRANGEMENT



TRUTH TABLE

CS	OE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	25 X	mm ×	Not Selected	IsB, IsB1	High Z	
L	L	008 H	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	BSI L	Write	Icc	Din	Write Cycle (1)
L	L	Opt L	Write	Icc	Din	Write Cycle (2)

RECOMMENDED DC OPERATING CONDITIONS $(Ta = -40 \text{ to } +85^{\circ}\text{C})$

Item	Symbol	min	typ	max	Unit
C 1 V 1 100	Vcc 05	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	626 0	V
- 01	OI VIH	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	958 <u>+</u>	0.8	V

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V \pm 10\%$, GND=0V, $T_a=-40$ to $+85^{\circ}$ C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	ILI	V_{cc} =5.5V, V_{cc} =GND to V_{cc}		-	2	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH}, \ V_{I \neq 0} = \text{GND to } V_{CC}$		- ,	2	μΑ
Operating Power Supply	Icc	$\overline{\text{CS}} = V_{IL}, I_{I \sim 0} = 0 \text{mA}$	_	35	90	mA
Current	Icc1**	$V_{IH} = 3.5 \text{ V}, \ V_{IL} = 0.6 \text{ V}, \ I_{L/O} = 0 \text{ mA}$	_	30	_	mA
Average Operating Current	Icc 2	min. cycle, duty=100%	-	35	90	mA
Standby Power Supply	Isa	$\overline{\text{CS}} = V_{LH}$	_	4	20	mA
Current	Isbi	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, \ V_{in} \ge V_{CC} - 0.2 \text{V} \text{ or } V_{in} \le 0.2 \text{V}$	-	2	100	μΑ
0	Vol	IoL = 2.1mA	-	-	0.4	V
Output Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.4	_	_	V

^{* :} Vcc = 5V, Ta = 25°C

AC CHARACTERISTICS ($V_{cc}=5V \pm 10\%$, $T_a=-40 \text{ to } +85^{\circ}\text{C}$)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

Item	Symbol	HM61	HM6116LPI-2		HM6116LPI-3		HM6116LPI-4	
Item	Symbol	m in	max	min	max	min	max	Unit
Read Cycle Time	t RC	120	_	150	-	200		ns
Address Access Time	taa	_	120	_	150		200	ns
Chip Select Access Time	tacs	-	120		150	_	200	ns
Chip Selection to Output in Low Z	tclz	10	1 -	10	-	10	_	ns
Output Enable to Output Valid	t o E	_	80	Jan 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	100		120	ns
Output Enable to Output in Low Z	toLZ	10	MILLE M. LOS	10	-	10	_	ns
Chip Deselection to Output in High Z	t c H Z	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Output Hold from Address Change	tон	10	-	10	11.	10	_	ns



^{* * :} Reference Only

• WRITE CYCLE

WO P. Ref. Cycle	C 1 1/19	HM611	6LPI-2	HM61	16LPI-3	HM6116LPI-4		Unit
ltem daily	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	t wc	120	-	150	_	200	-	ns
Chip Selection to End of Write	tcw	70	-	90	-	120	1	ns
Address Valid to End of Write	t _{AW}	105	-	120	-	140	_	ns
Address Set Up Time	tas	20	-	20	_	20	-	ns
Write Pulse Width	twp	70	STORO	90	ARTHO	120	CVERN	ns
Write Recovery Time	twn	5	-	10	_	10	-	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	- 0	40	-	60	_	ns
Data Hold from Write Time	t DH	8.8.5	-	10	-	10	_	ns
Output Active from End of Write	tow	5		10	-	10	- 19	ns

EXAMPLE 11 CAPACITANCE (f=1)MHz, Ta=25°C

OE

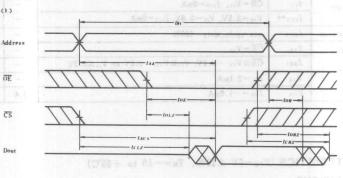
CS

Item	Symbol	Test Conditions	typ	max	Unit	
Input Capacitance	Cin	V OV anolitions) is	3 fuelos	5	pF	
Input/Output Capacitance	C1/0	$V_{LO} = 0 \text{V}$	5	7	pF	

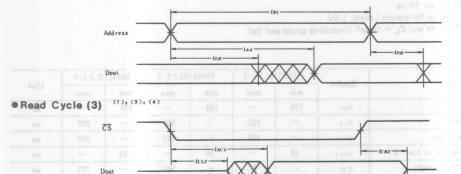
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

• Read Cycle (1) (1)

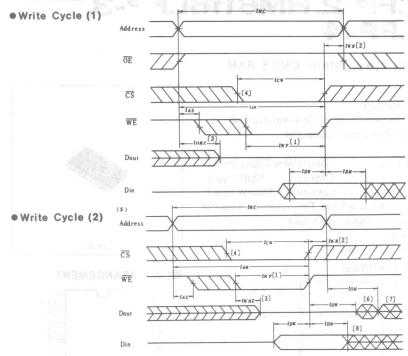


● Read Cycle (2) (1), (2), (4)



NOTES: 1. WE is High for Read Cycle.

- Device is continuously selected, \$\overline{\text{CS}}\$ = \$V_{IL}\$.
 Address Valid prior to or coincident with \$\overline{\text{CS}}\$ transition Low.
- 4. $\overline{OE} = V_{IL}$.



NOTES: 1. A write occurs during the overlap (twp) of a low CS and a low WE.

2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE}

going high to the end of write cycle.

3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE

transition, output remain in a high impedance

5. \overline{OE} is continuously low. $\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.

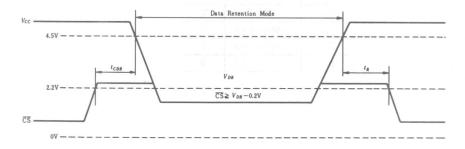
7. Dout is the read data of next address.
8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

LOW VCC DATA RETENTION CHARACTERISTICS (Ta = -40 to +85°C)

Item / w	Symbol Test Conditions		min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, \ V_{.\bullet} \ge V_{CC} - 0.2 \text{V} \text{ or } V_{.\bullet} \le 0.2 \text{V}$	2.0	_	_	V
Data Retention Current	ICCDR*	$V_{cc} = 3.0 \text{ V}, \ \overline{\text{CS}} \ge 2.8 \text{ V}, \ V_{.s} \ge 2.8 \text{ V or } -0.3 \text{ V} \le V_{.s} \le 0.2 \text{ V}$	-	-	50	μA
Chip Deselect to Data Retention Time	tcor	S. D W. (0	_	_	ns
Operation Recovery Time	t R	See Retention Waveform	t RC**	_	-	ns

^{*} $10 \,\mu\text{A}$ max at $Ta=-40\,\text{°C}$ to $+40\,\text{°C}$ $V_{IL} \,\text{min}=-0.3\,\text{V}$ * * $I_{RC}=\text{Read}$ Cycle Time.

● Low Vcc Data Retention Waveform



HM6116LFP-2, HM6116LFP-3, HM6116LFP-4

2048-word×8-bit High Speed Static CMOS RAM

FEATURES

- High Density Small-sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time

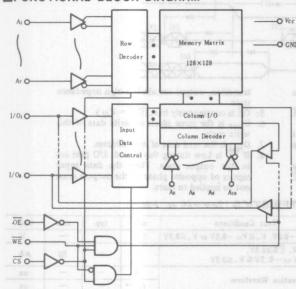
120ns/150ns/200ns (max.)

- Low Power Standby and Low Power Operation;
- Standby: $10\mu W$ (typ.) Operation: 160mW (typ.)
- Completely Static RAM:

No Clock nor Timing Strobe Required

- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

FUNCTIONAL BLOCK DIAGRAM



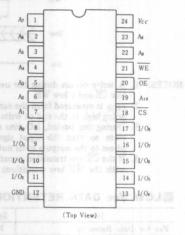
MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	Торг	0 to +70	°C
Storage Temperature	Tets	-55 to +125	°C
Temperature Under Bias	Thias	-10 to +85	°C
Power Dissipation	P_T	1.0	W

^{*} $V_{IN} \min = -1.5 \text{V (Pulse Width} \le 50 \text{ns)}$



PIN ARRANGEMENT



TRUTH TABLE

CS	OE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	sale × rein	×	Not Selected	IsB, IsB1	High Z	
L	- L 002	H	Read	Icc	Dout	Read Cycle (1)~(3)
L	(20 H	L-	Write	Icc	Din	Write Cycle (1)
L	- L 34	L	Write	301 Icc	Din	Write Cycle (2)

PRECOMMENDED DC OPERATING CONDITIONS $(Ta=0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	min	typ	max	Unit	
Supply Voltage	Vcc	4.5	5.0	5.5	V	
	GND	0	0	0	V	
0.0	V_{IH}	2.2	3.5	6.0	V	
Input Voltage	V_{IL}	-1.0*		0.8	V	

^{*} Pulse Width: 50ns, DC: V11 min = -0.3 V.

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, GND=0V, Ta=0 to $+70^{\circ}$ C)

	C 1.1	Test Conditions	HN	46116LF	P-2	HM6	6116LFP-	-3/-4	Unit
Item	Symbol Test Conditions		min	typ*	max	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	V_{CC} =5.5V, V_{in} =GND to V_{CC}	_		2	an 1 51	_	2	μΑ
Output Leakage Currnnt	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I < O} = \text{GND to } V_{CC}$	_	_	2	1	-	2	μΑ
O	Icc	$\overline{CS} = V_{IL}, I_{I=0} = 0 \text{mA}$	_	35	70	_	30	60	mA
Current Icci**		$V_{IH} = 3.5 \text{V}, V_{IL} = 0.6 \text{V},$ $I_{I=0} = 0 \text{mA}$	_	30	ļ	_	25	_	mA
Average Operating Current	Iccz	Min cycle, duty=100%	_	35	70	_	30	60	mA
C. II D. C. I	Isa	$\overline{\text{CS}} = V_{IH}$		4	12	_	4	12	mA
Current		$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{in} \ge V_{cc}$ -0.2V or $V_{in} \le 0.2 \text{V}$	1-1	-2	50	_	2	50	μΑ
History	17	$I_{OL} = 4 \text{mA}$	-	_	0.4	-	_	_	V
Output Voltage	$I_{OL} = 2.1 \text{mA}$			_	1./-		_	0.4	\ \
	Von	$I_{OH} = -1.0 \text{mA}$	2.4	-	_	2.4	_	_	V

^{* :} $V_{CC} = 5V$, $Ta = 25^{\circ}C$

EAC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and \mathcal{C}_L = 100pF (including scope and jig)

• READ CYCLE

Ta	Cll	HM611	6LFP-2	HM6116LFP-3		HM6116LFP-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	trc	120	-	150		200	_	ns
Address Access Time	taa	-)	120		150	_	200	ns
Chip Select Access Time	tacs	-	120	-	150	_	200	ns
Chip Selection to Output in Low Z	tclz	10	for Read	15	7. J_88	15	_	ns
Output Enable to Output Valid	toE	D-9123(5)	80	O ET DOLLA	100	_	120	ns
Output Enable to Output in Low Z	tolz	10	-	15	-	15	-	ns
Chip deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Output Hold from Address Change	t _{OH}	10	_	15	_	15	_	ns



^{* * :} Reference Only

• WRITE CYCLE

TAO I Ball Cycle	Symbol	HM611	6LFP-2	HM611	HM6116LFP-3		6LFP-4	Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	- ban	150	+	200	-	ns
Chip Selection to End of Write	tcw	70	-print	90		120	-	ns
Address Valid to End of Write	taw	105	-6134.)	120	-4	140	_	ns
Address Set Up Time	tas	20	-	20	-	20	_	ns
Write Pulse Width	twp	70	PENTIAN	90	A DETON	120	CONTRACTOR	ns
Write Recovery Time	twn	5		10	-	10	-	ns
Output Disable to Output in High Z	t onz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	_ UV	40	_	60		ns
Data Hold from Write Time	t _{DH}	5		10	-	10	- 1554	ns
Output Active from End of Write	tow	5	_	10	_	10		ns

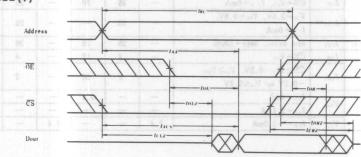
ECAPACITANCE $(f=1 \text{MHz}, Ta=25^{\circ}\text{C})$

Item	Symbol	Test Conditions	typ	max	Unit	
Input Capacitance	Cin	Vin=0V	3	5	pF	
Input/Output Capacitance	Ciro	$V_{I=0}=0$ V	5	7	pF	

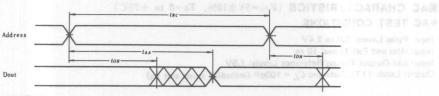
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

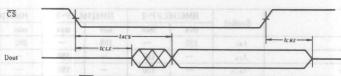
•READ CYCLE (1)(1)



•READ CYCLE (3)(1)(3)(4)

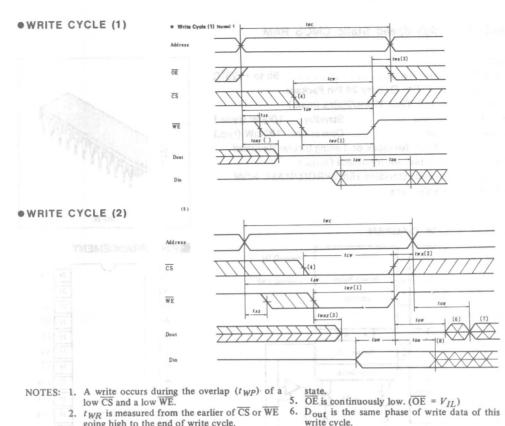


• READ CYCLE (2)(1)(2)(4)



- NOTES: 1. WE is High for Read Cycle
 2. Device is continuously selected, $\overline{CS} = V_{IL}$ 3. Address Valid prior to or coincident with \overline{CS} transition Low.

 - 4. $\overline{OE} = V_{IL}$.



- t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
 During this period, I/O pins are in the output
- During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

 7. Dout is the read data of next address.

 8. If CS is Low during this period, I/O pins are in the output state. Then the data input
- 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance

- write cycle.
- signals of opposite phase to the outputs must not be applied to them.

■LOW V_{cc} DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Item Symbol Test Conditions		min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V}$ $V_{IN} \ge V_{cc} - 0.2\text{V or } V_{IN} \le 0.2\text{V}$	2.0	_	_	V
tata Retention Current I_{CCDR}^{\bullet} V_{CC} -3.0V, $\overline{CS} \ge 2.8$ V $V_{IN} \ge 2.8$ V or $V_{IN} \le 0.2$ V		-	_	30	μΑ	
Chip Deselect to Data Retention Time	tcor	S P W . f	0	_		ns
Operation Recovery Time	t _R	See Retention Waveform	**tRC	_		ns

^{*} $V_{IL} \min = -0.3 \text{ V}, 10 \,\mu\text{A} \max (\text{at } T_a = 0 \text{ to } +40 \,\text{°C})$

** tRC-Read Cycle Time.

●Low Vcc DATA RETENTION WAVEFORM

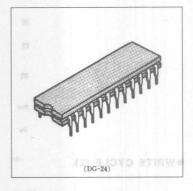


HM6116K-3, HM6116K-4

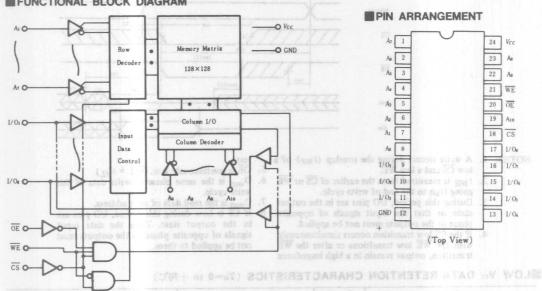
2048-word × 8-bit High Speed Static CMOS RAM

FEATURES

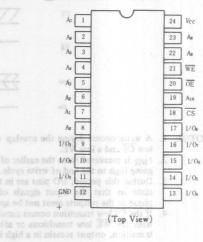
- Industrial Temperature Range 55 to +125°C
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation
 - Standby: 100µW (type.) Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time



FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



MADSOLUTE MAXIMUM RATINGS

Ass. Item	Symbol	Rating	Unit	Recon	Daka Retention Coverns
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V	8401	
Operating Temperature	Topr	-55 to +125	°C	11	Operation Recovery 1) us
Storage Temperature	(5.0)	6 Ver min - 0.3V, 10 - A max (at Ta-6 to +40%)			
Power Dissipation	P_T	1.0	W		b & reprofited Cycle Title
Pulse Width 50ng : -1 5V			- 8	TRO REVO	LOW VE DATA RETENTION WA

^{*} Pulse Width 50ns: -1.5V

TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	I_{SB} , I_{SB1}	High Z	
L	L	Н .	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	L	Write	I_{cc}	Din	Write Cycle(1)
L	L	L	Write	Icc	Din	Write Cycle (2)

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to $+70^{\circ}$ C)

Item Item	Symbol	min	typ	max	Unit
EBHS 0	V _{cc}	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	v
AG .	VIH	2.2	3.5	6.0	v
Input Voltage	VIL	-1.0*	-	0.8	V

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V\pm10\%$, GND=0V, $T_a=-55\sim+125^{\circ}C$)

		m . 0 . V.			J. 4008835	Y7. 14
Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	V_{cc} =5.5V, V_{in} =GND to V_{cc}	-	L Ten	10	μА
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{IZO} = \text{GND to } V_{CC}$	adirW 1	Controll building	10	μА
	I_{cc}	$\overline{\mathrm{CS}} = V_{IL}, \ I_{I \wedge O} = 0 \mathrm{mA}$	-	35	90	mA
Operating Power Supply Current	Icc1 **	V_{IB} = 3.5V, V_{IL} = 0.6V, $I_{I/o}$ = 0 mA	HMI =	30	ACITAS II	mA
Average Operating Current	Iccz	Min. cycle, duty=100%	-	35	90	mA
	I_{SB}	$\overline{\text{CS}} = V_{IH}$	M. was been	4	20	mA
Standby Power Supply Current	I_{SB1}	$CS \ge V_{CC} - 0.2V$, $V_{ia} \ge V_{CC}$ -0.2V or $V_{ia} \le 0.2V$	- 1,45	0.02	2	mA
0	Vol	I _{OL} =2.1mA	-	(1)	0.4	v
Output Voltage	V_{OH}	$I_{OH} = -1.0 \text{mA}$	2.4	_	_	V

^{*} Vcc-5V, Ta-25°C

EAC CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = -55$ to +125°C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100pF$ (including scope and jig)

• READ CYCLE

Item	C1	HM61	116K-3	HM61	16K-4	Unit	
Item	Symbol	min	max	min	max	Unit	
Read Cycle Time	t _{RC}	150	_	200	- 11	ns	
Address Access Time	tAA		150		200	ns	
Chip Select Access Time	tACS		150		200	ns	
Chip Selection to Output in Low Z	tcLZ	10	-	10	Dog	ns	
Output Enable to Output Valid	t OE		100	-	120	ns	
Output Enable to Output in Low Z	t olz	10	-	10	(c) (d)	ns	
Chip Deselection to Output in High Z	t _{CHZ}	0	50	0	60	ns	
Chip Disable to Output in High Z	t ohz	0	50	0	60	ns	
Output Hold from Address Change	t OH	10	- kral	10	- 1	ns	

^{**} Reference Only

• WRITE CYCLE

Item	Symbol	HM61	16K-3	HM6	116K-4	Unit	
Item 2	Symbol	min	max	min	max	Ont	
Write Cycle Time	twc	150	900	200		ns	
Chip Selection to End of Write	tcw	90		120	_	ns	
Address Valid to End of Write	t _{AW}	120	77.	140	- 11	ns	
Address Set Up Time	tAS	20	254	20		ns	
Write Pulse Width	t _{WP}	90	-	120	1 A TO 100	ns	
Write Recovery Time	t _{WR}	10	nero l as	10	MATTA GROOM	ns	
Output Disable to Output in High Z	tonz	0	50	0	60	ns	
Write to Output in High Z	twHz	329 0	60	0	60	ns	
Data to Write Time Overlap	t _{DW}	40	V2-5.5	60	Carreal	ns	
Data Hold from Write Time	t _{DH}	100-	$\overline{GS} = V_{DR}$	10		ns	
Output Active from End of Write	tow	10	Deg Al	10		ns	

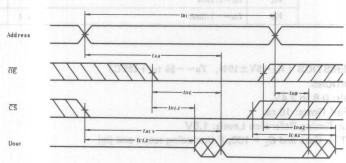
ECAPACITANCE $(f=1MHz, Ta=25^{\circ}C)$

Item	Symbol	Test Conditions	typ	max	Unit	
Input Capacitance	Cin	V., - 0 V	3	5	pF	
Input/Output Capacitance	$C_{\nu o}$	$V_{l,0} = 0 \text{V}$	5	7	pF	

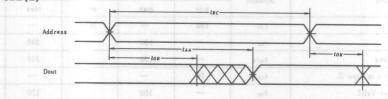
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

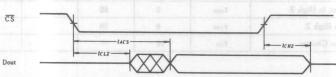
• READ CYCLE (1) (1)



• READ CYCLE (2) (1) (2) (4)



• READ CYCLE (3) (1)(3)(4)



NOTES: 1. WE is High for Read Cycle.

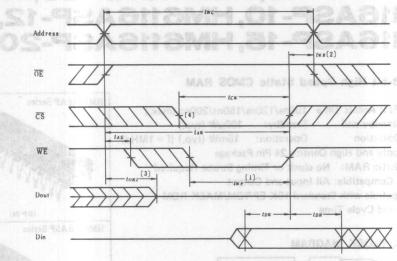
2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.

3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low.

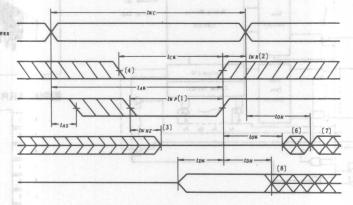
4. $\overline{\text{OE}} = V_{IL}$.



WRITE CYCLE (1)



• WRITE CYCLE (2) (5)



Din

CS

WE

- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.

 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
 - 5. \overline{OE} is continuously low. $(\overline{OE} = V_{IL})$ 6. Dout is the same phase of write data of this write cycle.

 - D_{out} is the read data of next address.

 If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6116AP-10, HM6116AP-12, HM6116AP-15, HM6116AP-20, 11 3 JOY 3 THEN HM6116ASP-10, HM6116ASP-12, HM6116ASP-15, HM6116ASP-20

2048-word×8-bit High Speed Static CMOS RAM

FURTURES

- High speed: Fast Access Time 100ns/120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (typ.) Low Power Operation

 - Operation: 15mW (typ.) (f = 1MHz)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

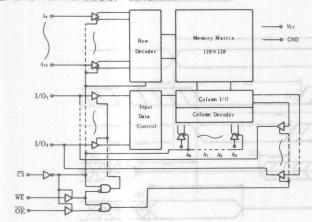
HM6116AP Series

HM6116ASP Series



(DP-24A)

FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS and a to (quart) qualitated with gallering and analysis still

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	Vrisia	-0.5° to +7.0	V	
Operating Temperature	Top.	0 to +70	.C	
Storage Temperature	Teta	-55 to +125	.C	
Temperature Under Bias	These	-10 to +85	°C	
Power Dissipation	P_{τ}	(1.0	W	

^{*} Pulse Width 50ns: -1.5V

PIN ARRANGEMENT

A7	1	T-11	24	Vce
As	2		23	As
	3		22	An
10	4		21	WI
As	5.		20	ŌĒ
Az	6		19	A10
Aı	7		18	CS
Ao	- 8		17	1/0
/O1	9		16	1/0
/Oz	10		15	1/0
1/01	11		14	1/0
IND	12		13	1/0

(Top View)

TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, IsBI	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

TRECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item Vindi Land	Symbol	min ii	typ	max	Unit	
C I WINE Xuan	Vcc	4.5	5.0	5.5	V	
Supply Voltage	GND	0	0	0	V	
120 - 120 - ns	VIH	2.2	3.5	6.0	V	
Input Voltage	VIL	-1.0*	WAT +	0.8	V	

^{*} Pulse Width: 50ns, DC: Vu min = -0.3V

DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, GND=0V, Ta=0 to +70°C)

200 L D3	20 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1														
an 1, 03	0 1 1	Test Conditions	НМ6	116AP/A	SP-10	НМ6	116AP/A	ASP-12	НМ6	116AP/A	ASP-15	HM6116AP/ASP-20			77-14
Item	Symbol	1 Test Conditions		typ*	max	min	typ*	max	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	V_{CC} =5.5V, V_{in} =GND to V_{CC}	1 0		2	0		2	-	atitle	2	erenik el est	from the	2	μА
Output Leakage Current	I _{LO}	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I/O} = \text{GND to } V_{CC}$	-	-	2	-	-	2	(= n')	īsH	2	75	MĀT	2	μА
Operating Power	Icc	$\overline{\text{CS}} = V_{IL}, I_{I/O} = 0 \text{mA}$ $V_{in} = V_{IH} \text{ or } V_{IL}$	-	5	15	vesT Ve	5	15	Symb	5	15	-	5	15	mA
Supply Current	I _{CC1}	I_{CC1} $V_{IH}=V_{CC}, V_{IL}=0V,$ $\overline{CS}=V_{IL},$ $I_{I/O}=0$ mA, $f=1$ MHz	-	3	6	76	3	6	65 65 8	3	6	eridine pre si	3	6	mA
Average Operating Current	I _{CC2}	min. cycle, duty=100%	-	40	70	-	35	60	_	25	45	1931	20	35	mA
Standby Power	ISB	CS= V _{IH}	-	1	4	-	1	4	-	1	4	-	1	4	mA
Supply Current	I _{SB1}	CS≥ V _{CC} -0.2V		0.02	2		0.02	2		0.02	2	-	0.02	2	mA
	VOL	I _{OL} =4mA	-		0.4	-	-	0.4	-	25%	0.4	-	-	0.4	V
Output Voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	A	2.4	_	-	2.4	-	-	2.4	-	_	v

^{*} Vcc=5V, Ta=25°C

EAC CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = 0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item	Symbol	HM6116AP/ ASP-10		HM6116AP/ ASP-12		HM6116AP/ ASP-15		HM6116AP/ ASP-20		Unit	
	-	min	max	min	max	min	max	min	max	Om	
Read Cycle Time	tRC	100		120		150	_	200	_	ns	
Address Access Time	t _{AA}	KAZ	100	-	120	-	150	-	200	ns	
Chip Select Access Time	tACS		100		120	-	150	-	200	ns	
Chip Selection to Output in Low Z	tCLZ	10	-	10	-	10	CAST CO.	10	_	ns	
Output Enable to Output Valid	tOE	-	50		55		60		70	ns	
Output Enable to Output in Low Z	tolz	10	-	10	-	10	_CS	10	-	ns	
Chip Deselection to Output in High Z	t _{CHZ}	0	40	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	toHZ	0	40	0	40	0	50	0	60	ns	
Output Hold from Address Change	t _{OH}	10	XX	10	_	15	tage?	20	_	ns	

1. Davice is combinuously schooled, CS = V_{II}

• WRITE CYCLE

Item a a	Symbol		16AP/ P-10		16 AP/ P-12		116AP/ P-15		16 AP/ P-20	Unit
Item a.a	Bymoor	min	max	min	max	min	max	min	max	Ome
Write Cycle Time	twc	100	-	120	-	150	_	200	-	ns
Chip Selection to End of Write	tcw	65	-	70	-	90	-	120	-	ns
Address Valid to End of Write	tAW	80	-	105	-	120	-	140		ns
Address Set Up Time	tAS	0	-	0	-	0	-	0	-	ns
Write Pulse Width	twp	60	-	70	-	80	-	100	-	ns
Write Recovery Time	twR	0	No. Ten S	0	RESTRICT	0	1 17 kg c	0	iosan.	ns
Output Disable to Output in High Z	toHZ	0	40	0	40	0	50	0	60	ns
Write to Output in High Z	twHZ	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	tDW	30	78 12 8	35	-	40	-	50	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	G M D≈	0	7.00	0	No.	ns
Output Active from End of Write	tow	10	-	10	-	10	Von.	10	-	ns

ERECOMMENDED DO OPERATING CONDITIONS (Ta-8 to +70°C)

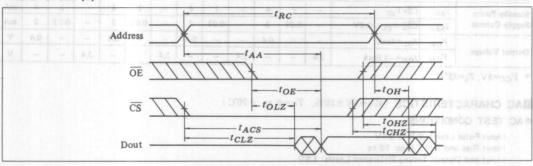
ECAPACITANCE $(f=1MHz, Ta=25^{\circ}C)$

Am Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	V.,-0V	3 70 %	5	pF
Input/Output Capacitance	Cvo	V10-0V	VIII-5 V	7	pF

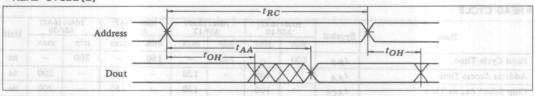
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

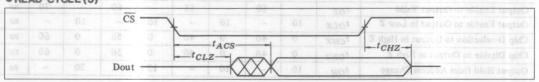
• READ CYCLE (1) (1)



● READ CYCLE (2) (1)(2)(4)



• READ CYCLE (3) (1)(3)(4)



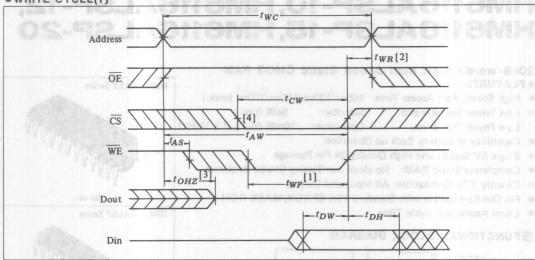
NOTES: 1. WE is High for Read Cycle.

- Device is continuously selected, S = V_{IL}.
 Address Valid prior to or coincident with S transition Low.

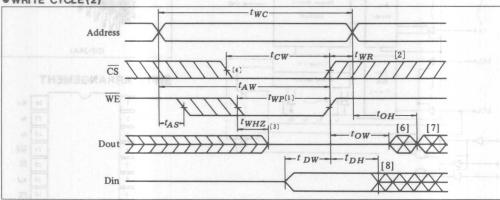
4. $\overline{OE} = V_{IL}$.







• WRITE CYCLE (2) (5)



- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$. 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

 - pedance state.
 OE is continuously low. (OE = V_{IL})
 Dout is the same phase of write data of this write cycle.
 Dout is the read data of next address.
 If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be capiled to them. not be applied to them.

HM6116ALP-10, HM6116ALP-12, HM6116ALP-15, HM6116ALP-20, HM6116ALSP-10, HM6116ALSP-12, HM6116ALSP-15, HM6116ALSP-20

2048-word×8-bit High Speed Static CMOS RAM

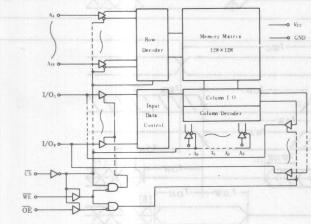
- **FEATURES**
- High Speed: Fast Access Time 100ns/120ns/150ns/200ns (max.)
- Low Power Standby and Standby:

5μW (typ.)

Low Power Operation; Operation: 10mW (typ.) (f = 1MHz)

- · Capability of Battery Back up Operation
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



MABSOLUTE MAXIMUM RATINGS

Item bns 033	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V.T	-0.5* to +7.0	V
Operating Temperature	T.p.	0 to +70	°C
Storage Temperature	Teta	-55 to +125	°C
Temperature Under Bias	T	-10 to +85	°C
Power Dissipation	P_T	1.0	W

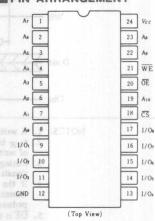
HM6116ALP Series



HM6116ALSP Series



PIN ARRANGEMENT



TRUTH TABLE and latter out in the output of a before and and and

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, IsBı	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
27 1 1 000 1/2	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	. 0	way 0	MinW to 0 and on a	oussi V
20 - 160 - 05	Vin	2.2	3.5	6.0	V V
Input Voltage	VIL	-1.0*	287 -	0.8	V

^{*} Pulse Width: 50ns, DC: VIL min = -0.3V

DC AND OPERATING CHARACTERISTICS (Vcc-5V ±10%, GND-0V, Ta-0 to +70°C)

86 08	Symbol	Test Conditions	Н	M6116A ALSP-1		Н	M6116A ALSP-1			M6116A ALSP-1		Н	M6116A ALSP-2		Unit
Item .	Symbol	Test Conditions	min	typ*	max	min	typ*	max	min	typ*	max	min	typ*	max	vect
Input Leakage Current	$ I_{LI} $	V_{CC} =5.5V, V_{in} =GND to V_{CC}	-0	-	2	-01	-	2	-	e <u>ii</u> rii	2	E _10	l gib	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I/O} = \text{GND to } V_{CC}$	_	-	2	-	-	2	-0	sHM	2	30V	ATE	2	μA
Operating Power	Icc	$\overline{\text{CS}}=V_{IL}, I_{I/O}=0\text{mA}$ $V_{in}=V_{IH} \text{ or } V_{IL}$	-	4	12	-	4	12	John O	4	12	_	4	12	mA
Supply Current	I _{CC1}	$\frac{V_{IH}=V_{CC}, \ V_{IL}=0\text{V},}{\overline{\text{CS}}=V_{IL},}$ $I_{I/O}=0\text{mA}, f=1\text{MHz}$		2	5	-	2	5	Co. co	2	5	egapea c	2	5	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	-	35	60	-	30	50	-	20	40	(1)	15	30	mA
Standby Power	I_{SB}	$\overline{\text{CS}} = V_{IH}$	-	0.5	3	-	0.5	3	-	0.5	3	I.T	0.5	3	mA
Supply Current	I _{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2\text{V}$	_	1	50	3	1	50	-	1	50	-	1	50	μА
Outant Valtara	VOL	I _{OL} =4mA	-	-	0.4	-	-	0.4	2/	-	0.4	PAG.	-	0.4	V
Output Voltage	VOH	I _{OH} =-1.0mA	2.4	-	-	2.4	-	-	2.4	-	-	2.4	-	-	V

^{* :} $V_{CC}=5V$, $T_a=25^{\circ}C$

■AC CHARACTERISTICS (Vcc=5V ±10%, Ta=0 to +70°C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item	Symbol		16ALP/ SP-10		16ALP/ SP-12		16ALP/ SP-15	HM611 ALS	6ALP/ P-20	Unit
Itom	Symoon	min	max	min	max	min	max	min	max	Onit
Read Cycle Time	tRC	100	-	120	-	150	-	200	-	ns
Address Access Time	tAA		100		120	-4-	150	_	200	ns
Chip Select Access Time	tACS		100	-	120		150	-	200	ns
Chip Selection to Output in Low Z	tCLZ	10	CXX	10	-	10	-30	10	-	ns
Output Enable to Output Valid	tOE		50	_	55	-	60	-	70	ns
Output Enable to Output in Low Z	tolz	10	-	10	-	10	_	10	a Dyd	ns
Chip Deselection to Output in High Z	t _{CHZ}	0	40	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	toHZ	0	40	0	40	0	50	0	60	ns
Output Hold from Address Change	toH	10		10		15	_	20	-	ns

• WRITE CYCLE

Item	Symbol		16ALP/ P-10		16ALP/ SP-12		16ALP/ SP-15		6ALP/ P-20	Unit
Half Item (new	Dymoor	min	max	min	max	min	max	min	max	Ome
Write Cycle Time	twc	100	-	120	-	150	-	200	estay.	ns
Chip Selection to End of Write	t _{CW}	65	-	70	+	90	-	120	-	ns
Address Valid to End of Write	tAW	80	-	105	+	120	-	140	-	ns
Address Set Up Time	tAS	· 0	-	0	-	0	-	0	380716	ns
Write Pulse Width	twp	60	-	70	-	80	-	100	4	ns
Write Recovery Time	twR	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High Z	toHZ	0	40	0	40	0	50	0	60	ns
Write to Output in High Z	twHZ	0	30	0	35	0	40	.0	50	ns
Data to Write Time Overlap	t _{DW}	30	- 72	35	- 300	40	107 - 10	50		ns
Data Hold from Write Time	t _{DH}	- 0	2000	0	-	0	11-1	0	-	ns
Output Active from End of Write	tow	10		10	QMD*,	10	300 ·	10	58,6269	ns

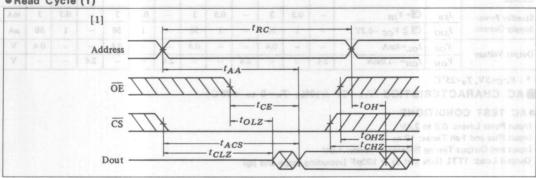
EXAMPLE 1.1 CAPACITANCE $(f=1 \text{MHz}, Ta=25^{\circ}\text{C})$

ltem	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	V., - 0V	3 4	5	pF
Input/Output Capacitance	Ciro	V1 0 = 0 V	W05 114 100	7	pF

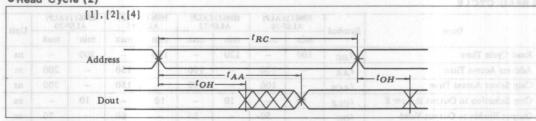
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

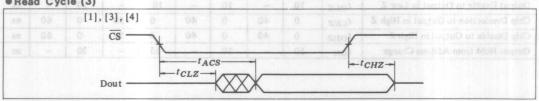
Read Cycle (1)



• Read Cycle (2)



Read Cycle (3)



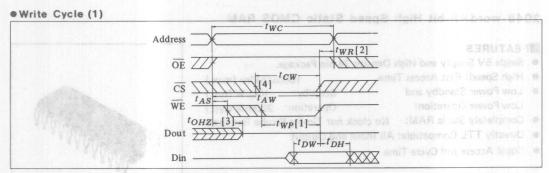
NOTES: 1. WE is High for Read Cycle.

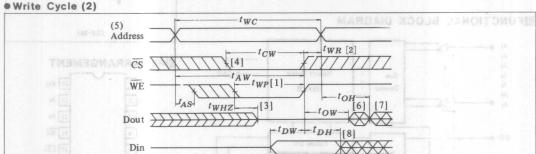
2. Device is continuously selected, $\overline{CS} = V_{IL}$.

3. Address Valid prior to or coincident with CS transition Low.

4. $\overline{OE} = V_{IL}$. 160







- NOTES: 1. A write occurs during the overlap (twp) of a low CS and a low WE.
 - 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE

transition, output remain in a high impedance

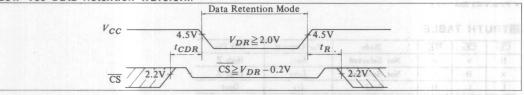
- 5. \overline{OE} is continuously low. $\overline{OE} = V_{IL}$)
- 6. Dout is the same phase of write data of this write cycle.
- 7. Dout is the read data of next address.
 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

LOW VCC DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Conditions		min	typ	max	Unit
Vcc for Data Retention	VDR	CS≥Vcc -0.2V	Lodgered	2.0	-	el -	V
Data Retention Current	Iccor*	Vcc = 3.0 V, CS ≥ 2.8 V	- 17	(BIS 01)	wija ja ti	30	μΑ
Chip Deselect to Data Retention Time	tcor	W 0.1	19	0	_	eo Laginsi	ns
Operation Recovery Time	t R	See Retention Waveform		t RC **		ried a T g	ns

^{* 10} μ A max at Ta=0°C to ± 40 °C, V_{IL} min = -0.3 V * * t_{RL} = Read Cycle Time.

● Low Vcc Data Retention Waveform



HM6117P-3, HM6117P-4

2048-word×8-bit High Speed Static CMOS RAM

FEATURES

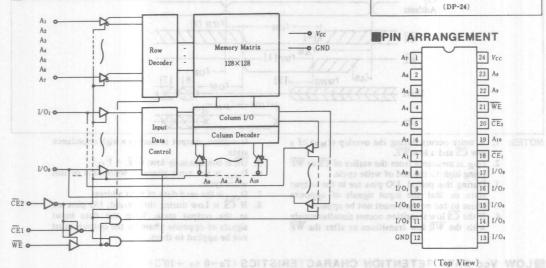
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time

150ns/200ns (max.)

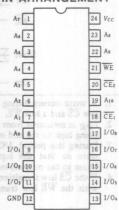
- Low Power Standby and
- Standby: 100μW (typ.)
- Low Power Operation: Completely Static RAM: No clock nor Timing Strobe Required
 - Operation: 200mW (typ.)
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

PARAPARAPARA (DP-24)

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



e Low Vcc Data Relention Wavelerm

MABSOLUTE MAXIMUM RATINGS

Item - 8	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Talg	-55 to +125	°C
Temperature Under Bias	Thias	-10 to +85	°C

^{*} Pulse width 50ns: -1.5V

TRUTH TABLE

CE ₁	CE ₂	WE	Mode	Vcc Current	I/O Pin
Н	- ×	×	Not Selected	IccLi	High Z
×	Н	×	Not Selected	Iccl2	High Z
L	L	Н	Read	Icc	Dout
L	L	L	Write	Icc	Din

■RECOMMENDED DC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	444 0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	VIL	-1.0*	14/11/1	0.8	V

^{*} Pulse width: 50ns, DC: VILNIS = -0.3V

DC AND OPERATING CHARACTERISTICS ($T_a=0$ °C to +70°C, $V_{cc}=5$ V ± 10 %, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	V_{in} =GND to V_{CC}	-	-	10	μΑ
Output Leakage Current	I _{LO}	$\overline{\text{CE}}_1 = V_{IH} \text{ or } \overline{\text{CE}}_2 = V_{IH}$ $V_{I < O} = \text{GND to } V_{CC}$	elgiH <u>si</u> JW	I 23row	10	μΑ
Operating Power Supply Current: DC	Icc	$\overline{CE}_1 = \overline{CE}_2 = V_{IL}, I_{I \sim O} = 0 \text{ mA}$	-	40	80	mA
Average Operating Current	Icci	Min cycle, duty=100% $\overline{CE}_1 = V_{IL}, \overline{CE}_2 = V_{IL}$	-	40	80	mA
Standby Power Supply Current (1): DC	IccL1*	$\overline{CE}_1 \ge V_{CC} - 0.2V,$ $V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$		0.02	2	mA
Standby Power Supply Current (2): DC	Icc12*	$\overline{CE}_2 \ge V_{CC} - 0.2V$	-	0.02	2	mA
Output low Voltage	Vol	IoL = 2.1mA	-	_	0.4	V
Output High Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.4	-	194 T. W	V

Notes: 1) Typical limits are at V_{CC} =5.0V, Ta=+25°C 2) *: V_{ILmin} =-0.3V

ECAPACITANCE $(Ta=25^{\circ}C, f=1.0MHz)$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	CIN	$V_{IN}=0$ V	JOYO33TIAV	5 0 1	pF
Input/Output Capacitance	Ciro	$V_{L,o} = 0 \text{ V}$	5	7	pF

Note) This parameter is sampled and not 100% tested.

EAC CHARACTERISTICS (Ta=0°C to +70°C, $V_{cc}=5$ V ± 10 % unless otherwise noted)

• AC TEST CONDITIONS

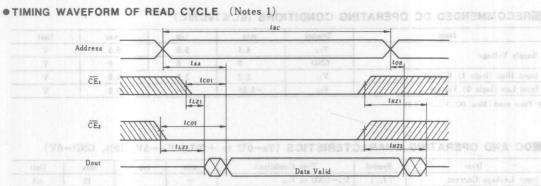
Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1 TTL Gate and C_L=100pF (including scope and jig)

• READ CYCLE

Item	Cumbal	HM61	17P-3	HM61	17P-4	Unit
Item	Symbol	min	max	min	max	Unit
Read Cycle Time	trc	150	_	200	_	ns
Address Access Time	LAA	icu C Ta	150	b mason s	200	ns
Chip Enable (CE1) to Output	tcoi	910 -	150	10 (44:1)	200	ns
Chip Enable (CE2) to Output	tcoz	TRAT	150	(W)	200	ns
Chip Enable (CE1) to Output in Low Z	tLZI	10	P(E) B1003	10	Mar Street	ns
Chip Enable (CE2) to Output in Low Z	tLZ2	10	CITTATION DATE	10	Total (III)	ns
Chip Disable (CE1) to Output in High Z	t _{HZ1}	под 0	70	0	80	ns
Chip Disable (CE2) to Output in High Z	t _{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t _{OH}	15	to has a	15	80007	ns

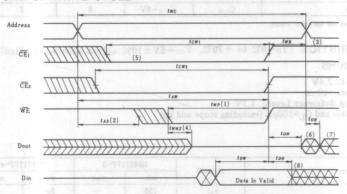


NOTES: 1. WE is High for Read Cycle.

• WRITE CYCLE

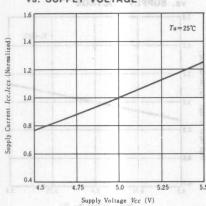
L.	Symbol	HM6117P-3		HM6117P-4		I I - i a	
Item	Symbol	min	max	min	max	Unit	
Write Cycle Time	twc	150	V=133_	200	-	ns	
Chip Enable (CE1) to End of Write	tcwi	100	15.53 <u>L</u>	120	A pales	ns	
Chip Enable (CE2) to End of Write	t cw2	110	-417	130		ns	
Address Set Up Time	tas	20	ester s	20	Gladnig	ns	
Address Valid to End of Write	tAW	130	_	150		ns	
Write Pulse Width	twp	100	5-10-50	120	- 7203	ns	
Write Recovery Time	twR	15	The Line	15	_92111	ns	
Write to Output in High Z	twHz	0	60	0	70	ns	
Data to Write Time Overlap	t _{DW}	50	_	60	-	ns	
Data Hold from Write Time	t _{DH}	20	-08/0 t-	20	e sz hiak	ns	
Output Active from End of Write	tow	10	-	10	- 110	ns	

TIMING WAVEFORM OF WRITE CYCLE

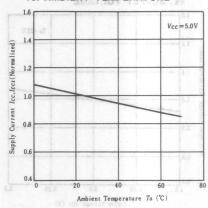


- NOTES: 1 A write occurs during the overlap (t_{WP}) of low \overline{CE}_1 , \overline{CE}_2 and \overline{WE} .
 - 2. t_{AS} is measured from the address changes to the biginning of the write.
 - 3. t_{WR} is measured from the earlier of \overline{CE}_1 , \overline{CE}_2 or \overline{WE} going high to the end/of write cycle.
- 4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 5. If the \overline{CE}_1 or \overline{CE}_2 low transition occurs simultaneously with the WE low transitions or after the WE transitions, output remain in a high impedance state.
- 6. Dout is the same phase of write data of this write cycle.
- 7. Dout is the read data of next address.
- 8. If $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

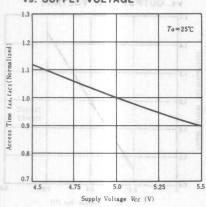
SUPPLY CURRENT vs. SUPPLY VOLTAGE



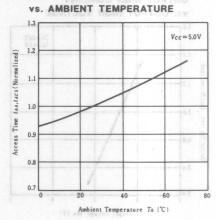
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



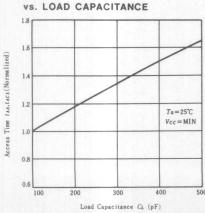
ACCESS TIME
vs. SUPPLY VOLTAGE



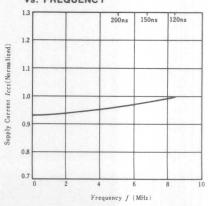
ACCESS TIME



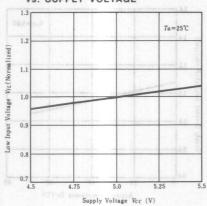
ACCESS TIME



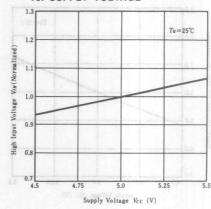
SUPPLY CURRENT vs. FREQUENCY



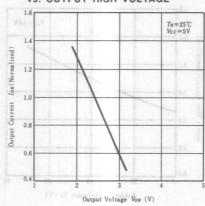
INPUT LOW VOLTAGE
vs. SUPPLY VOLTAGE



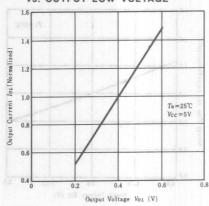
INPUT HIGH VOLTAGE
vs. SUPPLY VOLTAGE

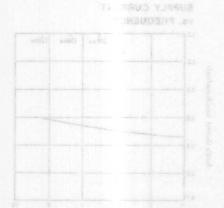


OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE







HM6117FP-3, HM6117FP-4

2048-word×8-bit High Speed Static CMOS RAM

FEATURES

- High Density Small Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time

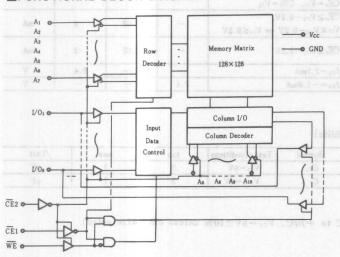
150ns/200ns (max.)

 Low Power Standby and Low Power Operation: Standby: 100µW (typ.) Operation: 200mW (typ.)

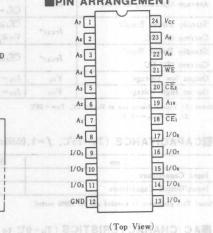
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time



FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



SAC TEST CONSTIQUE

MADSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit			
V_T	*-0.5 to +7.0	V			
P_T	1.0	W			
Topr	0 to +70	°C			
Teta	-55 to +125	°C			
Think	-10 to +85	ary .C			
	VT PT Topr	V_T *-0.5 to +7.0 P_T 1.0 T_{opr} 0 to +70 T_{stg} -55 to +125			

^{*} Pulse width 50ns: -1.5V

TRUTH TABLE

CE ₁	CE2	WE	Mode	Vcc Current	I/O Pin
Н	×	×	Not Selected	IccLi	High Z
×	Н	×	Not Selected	Iccli	High Z
L	L	Н	Read	Icc	Dout
L	L	L	Write	Icc	Din

TRECOMMENDED DC OPERATING CONDITIONS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Item	Symbol	OM min ises	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.2	3.5	6.0	V.
Input low (logic 0) Voltage	Vic of ten	-1.0*	fortelT and as	0.8	V

Thickness Reduced to a Half of Conventional Difference Signals Supply and Migh Density 24 pin Packago.

DC AND OPERATING CHARACTERISTICS (Ta=0°C to +70°C, $V_{cc}=5$ V ± 10 %, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current		Vin=GND to Vcc 12 printing	n doato ol/	NAME OF	10	μΑ
Output Leakage Current	ILO	$\overline{\text{CE}}_1 = V_{IH} \text{ or } \overline{\text{CE}}_2 = V_{IH}$ $V_{I \sim 0} = \text{GND to } V_{CC}$	ns zu <u>o</u> ni il	A tald <u>i</u> rso Ovela Tim	10	μA
Operating Power Supply Current: DC	Icc	$\overline{CE}_1 = \overline{CE}_2 = V_{IL}, I_{I=0} = 0 \text{mA}$		40	80	mA
Average Operating Current	Icci	Min cycle, duty=100% $\overline{CE}_1 = V_{IL}, \ \overline{CE}_2 = V_{IL}$	MARDA	40	80	mA
Standby Power Supply Current (1): DC	IccL1*	$\overline{CE}_1 \ge V_{CC} - 0.2V,$ $V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$		0.02	2	mA
Standby Power Supply Current (2): DC	Icc12*	CE2≥Vcc-0.2V	E	0.02	2	mA
Output low Voltage	Vol	IoL = 2.1mA	-	1-	0.4	→ V
Output High Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.4	-	-24	V

Notes: 1) Typical limits are at $V_{cc} = 5.0$ V, Ta = +25°C

ECAPACITANCE $(Ta=25^{\circ}C, f=1.0 \text{MHz})$

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	C ₁ o	$V_{I} = 0 \text{ V}$	5	7	pF

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (Ta=0°C to +70°C, $V_{cc}=5$ V ± 10 % unless otherwise noted)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

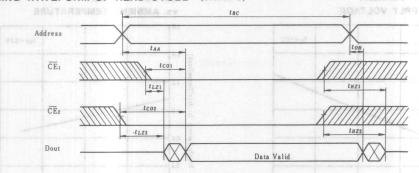
• READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit	
Item	Symbol	min	max	min	max	Unit	
Read Cycle Time	5 tRC 28+	150	100	200	Lister Birk	ns	
Address Access Time	taa	-	150	-	200	ns	
Chip Enable (CE1) to Output	tcoi	_	150	-	200	ns	
Chip Enable (CE2) to Output	tcoz	_	150	_	200	ns	
Chip Enable (\overline{CE}_1) to Output in Low Z	tLZI	10		10	rus-rs	ns	
Chip Enable (\overline{CE}_z) to Output in Low Z	tLZZ	10		10		ns	
Chip Disable (\overline{CE}_1) to Output in High Z	t _{HZ1}	0	70	0	80	ns	
Chip Disable (\overline{CE}_2) to Output in High Z	t _{HZ2}	0	70	0	80	ns	
Output Hold from Address Change	ton	15		15		ns	

^{*} Pulse width: 50ns, DC: VILINIA = -0.3V

^{2) * :} VILAIS = -0.3V

TIMING WAVEFORM OF READ CYCLE (Notes 1)

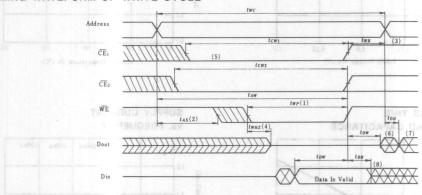


NOTES: 1. WE is High for Read Cycle.

• WRITE CYCLE

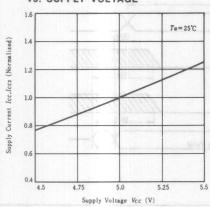
Item	Symbol	HM61	117P-3	HM6	117P-4	Unit
Item	Symbol	min	max	min	max	Unit
Write Cycle Time	twc	150	_	200		ns
Chip Enable (CE1) to End of Write	t c wı	100	-	120	NCC#68 18	ns
Chip Enable (CE2) to End of Write	t _{CW2}	110	- 3	130	18, SHEPLY	ns
Address Set Up Time	tas	20		20	E	ns
Address Valid to End of Write	taw	130	- 1	150	1 - 14	ns
Write Pulse Width	twp	100		120		ns
Write Recovery Time	twR	15	-	15	1 - 1	ns
Write to Output in High Z	twHZ	0	60	0	70	ns
Data to Write Time Overlap	tow	50	-	60	- 1	ns
Data Hold from Write Time	t _{DH}	20		20		ns
Output Active from End of Write	tow	10	_	10	- 1	ns

TIMING WAVEFORM OF WRITE CYCLE

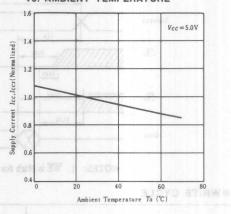


- NOTES: 1. A write occurs during the overlap (t_{WP}) of low \overline{CE}_{1} , \overline{CE}_{2} and \overline{WE}_{2} .
 - t_{AS} is measured from the address changes to the biginning of the write.
 - 3. t_{WR} is measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or \overline{WE} going high to the end/of write cycle.
- 4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 5. If the \overline{CE}_1 or \overline{CE}_2 low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transitions, output remain in a high im-
- pedance state.
- Dout is the same phase of write data of this write cycle.
- Dout is the read data of next address.
- If CE₁ and CE₂ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

SUPPLY CURRENT vs. SUPPLY VOLTAGE

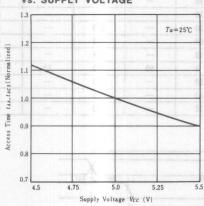


SUPPLY CURRENT vs. AMBIENT TEMPERATURE



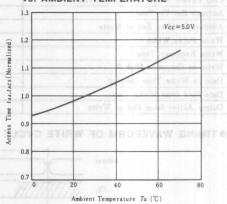
ACCESS TIME





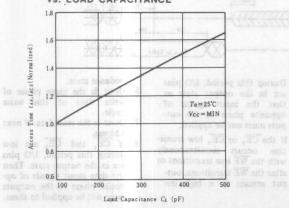
ACCESS TIME

VS. AMBIENT TEMPERATURE

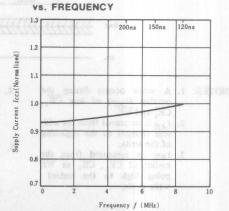


ACCESS TIME

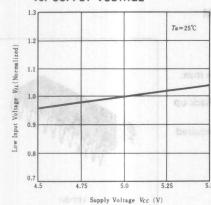
VS. LOAD CAPACITANCE



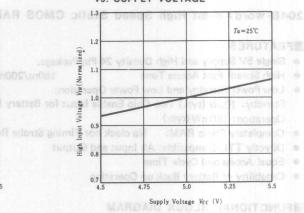
SUPPLY CURRENT.



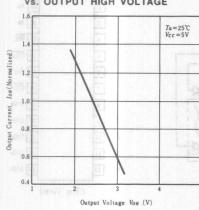
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



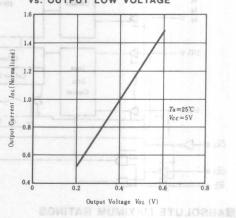
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



HM6117LP-3, HM6117LP-4

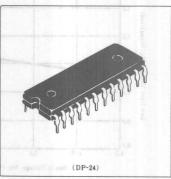
2048-word×8-bit High Speed Static CMOS RAM

FEATURES

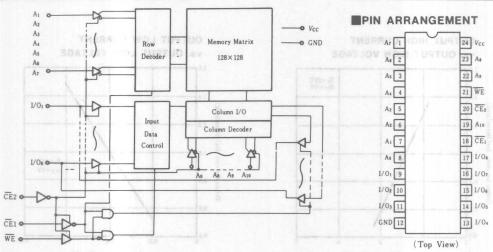
- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time

150ns/200ns max.

- Low Power Standby and Low Power Operation;
 Standby: 10µW (typ.) Two Chip Enable Input for Battery Back up
 Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation



FUNCTIONAL BLOCK DIAGRAM



MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V_T	*-0.5 to +7.0	V	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	
Temperature Under Bias	Thias	-10 to +85	°C	
Power Dissipation	P_T	1.0	·W	

^{*} Pulse width 50ns: -1.5V

TRUTH TABLE

\overline{CE}_1	CE ₂	WE	Mode Vcc Current		I/O Pin
Н	×	×	Not Selected	IccLi	High Z
×	Н	×	Not Selected	Not Selected Iccl2	
L	L	Н	Read	Icc	Dout
L	L	L	Write	Icc	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to+70°C)

Item	Symbol	min	typ	max	Unit
C 1 VI	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.2	3.5	6.0	V
Input low (logic 0) Voltage	VIL	-1.0*		0.8	V

^{*} Pulse Width: 50ns, DC: VILmin = -0.3V.

DC AND OPERATING CHARACTERISTICS ($Ta=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $Vcc=5\text{V}\pm10\%$, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	V _{IN} =GND to V _{CC}	-	_	2	μA
Output Leakage Current	ILO	$ \overline{CE}_1 - V_{IH} \text{ or } \overline{CE}_2 - V_{IH} \\ V_{I \neq 0} = \text{GND to } V_{CC} $		-	2	μA
Operating Power Supply Current: DC	Icc	$\overline{CE}_1 = \overline{CE}_2 = V_{IL}, I_{I \vee O} = 0 \text{mA}$	-	35	70	mA
Average Operating Current	Icci	Min cycle, duty=100% $\overline{CE}_1 = V_{IL}, \overline{CE}_2 = V_{IL}$	-	35	70	mA
Standby Power Supply Current (1): DC	IccL1*	$\overline{CE}_1 \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	-	2	50	μΑ
Standby Power Supply Current (2): DC	Icc12*	$\overline{\text{CE}}_2 \ge V_{CC} - 0.2\text{V}$	_	2 10	50	μΑ
Output low Voltage	Vol	$I_{OL}=2.1\text{mA}$	-	V	0.4	V
Output High Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.4	-	7.09	V

Notes: 1) Typical limits are at $V_{cc}=5.0$ V, Ta=+25°C

2) *: V_{ILnia} = -0.3V

ECAPACITANCE $(Ta=25^{\circ}C, f=1.0 \text{MHz})$

	Item	Symbol	Test Conditions	typ	max	Unit
Input Capaci	tance	Cin	$V_{IN}=0V$	3	5	pF
Input/Output	Capacitance	Civo	$V_{I \times O} = 0 \text{ V}$	5	7	pF

Note: 1) This parameter is sampled and not 100% tested.

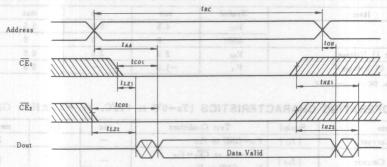
MAC CHARACTERISTICS ($Ta=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{cc}=5\text{V}\pm10\%$ unless otherwise noted)

• AC TEST CONDITIONS

• READ CYCLE

Item	Symbol	HM61	17LP-3	HM6117LP-4		Unit
Item	Symbol	min	max	min	max	Unit
Read Cycle Time	trc	150	-	200	_	ns
Address Access Time	taa	_	150		200	ns
Chip Enable (CE1) to Output	tcol	_	150	-	200	ns
Chip Enable (CE2) to Output	tcoz	ensu(T. A.	150	nub-various	200	ns
Chip Enable (CE1) to Output in Low Z	tLZI	10	177 sec	10	f. 1/15/10	ns
Chip Enable (CE2) to Output in Low Z	tLZ2	10	-	10	CHE ALC	ns
Chip Disable (CE1) to Output in High Z	t _{HZ1}	0	70	0	80	ns
Chip Disable (CE2) to Output in High Z	t _{HZ2}	0	70	0	80	ns
Output Hold from Address Change	ton.	15	mili Tracel	15		ns

TIMING WAVEFORM OF READ CYCLE (Notes 1) TIMING DATABLED OF TIMING WAVEFORM OF READ CYCLE (Notes 1)

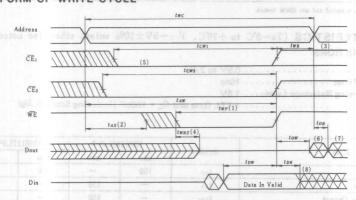


NOTES: 1. WE is High for Read Cycle.

• WRITE CYCLE

Ata 00	6.00	HM61	117LP-3	HM61	17LP-4	Unit
Item	Symbol	min	max	min	max	Unit
Write Cycle Time	twc	150	1/80 L	200	visues s	ns
Chip Enable (CE1) to End of Write	tcwi	100	1984 -	120	_100	ns
Chip Enable (CE2) to End of Write	tcwz	110	9.55	130	y Equip Si re	ns
Address Set Up Time	tas	20	-	20	- 30	ns
Address Valid to End of Write	taw	130	- 10°	150	<u> - 100 k 100</u>	ns
Write Pulse Width	twp	100	723 _ 30	120	4-1101	ns
Write Recovery Time	tw _R	15	<u> →</u> /20++	15	- 11 mm (1)	ns
Write to Output in High Z	twHz	0	60	0	70	ns
Data to Write Time Overlap	tow	50	1040 1	60	21/5/20 0.20	ns
Data Hold from Write Time	t _{DH}	20	1130011-0	20	N STEPPER	ns
Output Active from End of Write	tow	10	8	10	marl —	ns

TIMING WAVEFORM OF WRITE CYCLE



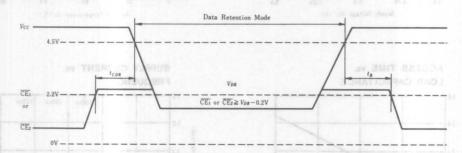
- NOTES: 1 A write occurs during the overlap (twp) of low \overline{CE}_1 , \overline{CE}_2 and \overline{WE} .
 - t_{AS} is measured from the address changes to the biginning of the write.
 - 3. t_{WR} is measured from the earlier of \overline{CE}_1 , \overline{CE}_2 or \overline{WE} going high to the end/of write cycle.
- During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 5. If the \overline{CE}_1 or \overline{CE}_2 low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transitions, output remain in a high impedance state.
- Dout is the same phase of write data of this write cycle.
- 7. Dout is the read data of next address.
- 8. If CE₁ and CE₂ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°Cto +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V _{CC} for Data Retention	V_{DR1}	$\overline{\text{CE}}_1 \ge V_{CC} - 0.2\text{V},$ $V_{IN} \ge V_{CC} - 0.2\text{V or } V_{IN} \le 0.2\text{V}$	2.0			V
Vcc for Data Retention	V_{DR2}	$\overline{CE}_2 \ge V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	ICCDR1	$V_{CC} = 3.0 \text{V}, \overline{\text{CE}}_1 \ge 2.8 \text{V},$ $V_{IN} \ge 2.8 \text{V} \text{ or } V_{IN} \le 0.2 \text{V}$	-	-	30*	μА
Data Retention Current	ICCDR2	$V_{cc}=3.0V$, $\overline{\text{CE}}_2 \ge V_{cc}-0.2V$		-	30*	μА
Chip Deselect to Data Retention Time	toor	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t _R			-	120	ns

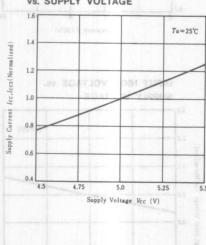
^{* 10} µA max at Ta=0°C to +40°C, VIL min=-0.3V

● LOW Vcc DATA RETENTION WAVEFORM

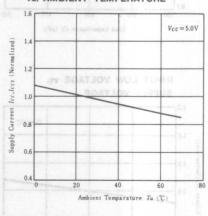


NOTE: 1. \overline{CE}_2 controls Address buffer, \overline{WE} buffer, \overline{CE}_1 buffer and D_{IN} buffer, If \overline{CE}_2 controls data retention mode, V_{IN} level (address, \overline{WE} , \overline{CE}_1 , $D_{I/O}$) can be in the high impedance state. If \overline{CE}_1 controls data retention mode, V_{IN} level (address, \overline{WE} , \overline{DE}_2 , $D_{I/O}$) must be $V_{IN} \ge V_{CC} - 0.2 V$ or $V_{IN} \le 0.2 V$.

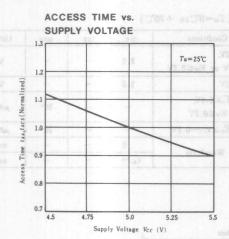
SUPPLY CURRENT vs. SUPPLY VOLTAGE

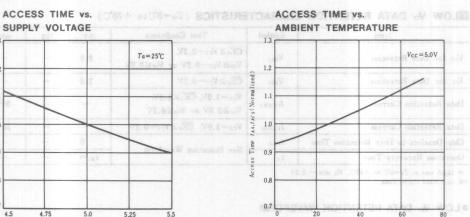


SUPPLY CURRENT vs. AMBIENT TEMPERATURE

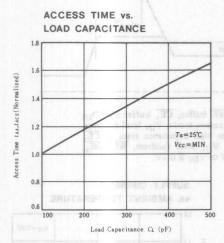


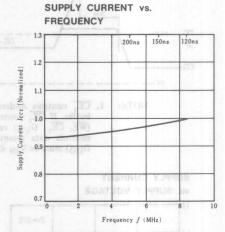
^{**} tRC=Read Cycle Time

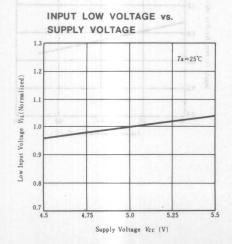


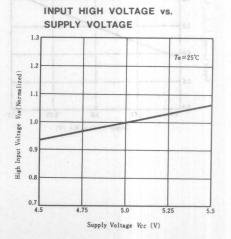


Ambient Temperature Ta (*C)

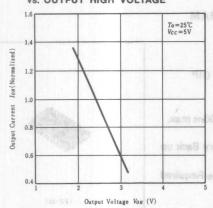




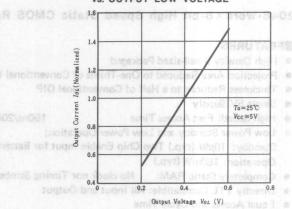




OUTPUT HIGH CURRENT
vs. OUTPUT HIGH VOLTAGE

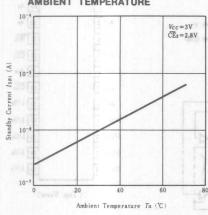


OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

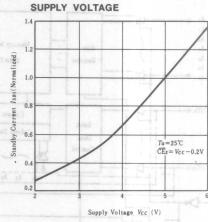


STAND-BY CURRENT vs.
AMBIENT TEMPERATURE

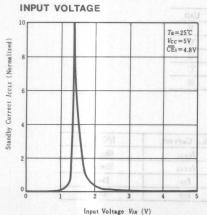
MINE BRANGEMENT



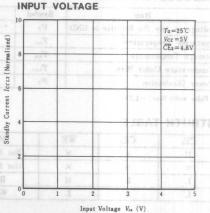
STAND-BY CURRENT vs.



STAND-BY CURRENT vs.



STAND-BY CURRENT VS. STUDIOS BAS



HM6117LFP-3, HM6117LFP-

2048-word×8-bit High Speed Static CMOS RAM

FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time

150ns/200ns max.

 Low Power Standby and Low Power Operation; Standby: 10µW (typ.) Two Chip Enable Input for Battery Back up

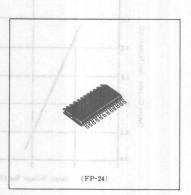
Operation: 180mW (typ.) Completely Static RAM:

No clock nor Timing Strobe Required

• Directly TTL Compatible: All Input and Output

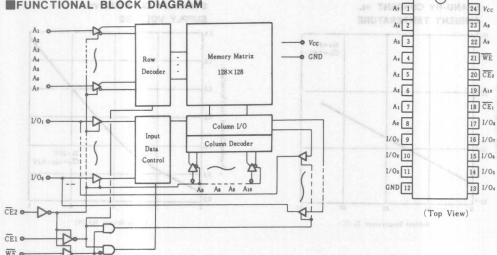
Equal Access and Cycle Time

Capability of Battery Back up Operation



PIN ARRANGEMENT





MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V_T	*-0.5 to +7.0	V	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tets	-55 to +125	°C	
Temperature Under Bias	Thias	-10 to +85	°C	
Power Dissipation	P_T	1.0	W	

^{*} Pulse width 50ns: -1.5V

TRUTH TABLE

CE ₁	CE ₂	WE	Mode	Vcc Current	I/O Pin
Н	×	×	Not Selected	IccLi	High Z
×	Н	×	Not Selected	IccL2	High Z
L	L	Н	Read	Icc	Dout
L	L	L	Write	Icc	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to+70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.2	3.5	6.0	V
Input low (logic 0) Voltage	VIL	-1.0*		0.8	V

^{*} Pulse Width: 50ns, DC: VILING = -0.3V.

DC AND OPERATING CHARACTERISTICS ($Ta=0^{\circ}C$ to $+70^{\circ}C$, $V_{cc}=5V\pm10\%$, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	V _{IN} =GND to V _{CC}	-	-	2	μA
Output Leakage Current	ILO	$\overline{CE}_1 = V_{IH}$ or $\overline{CE}_2 = V_{IH}$ $V_{IVO} = \text{GND to } V_{CC}$	ael dallit ei 3	W .I :ear	2	μΑ
Operating Power Supply Current: DC	Icc	$\overline{CE}_1 = \overline{CE}_2 = V_{IL}, I_{I = 0} = 0 \text{mA}$	-	35	70	mA
Average Operating Current	Icci	Min cycle, duty-100% $\overline{\text{CE}}_1 - V_{IL}, \ \overline{\text{CE}}_2 - V_{IL}$	-	35	70	mA
Standby Power Supply Current (1): DC	Icc Li*	$\overline{CE}_1 \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	-	2	50	μΑ
Standby Power Supply Current (2): DC	Icc12*	$\overline{\text{CE}}_{z} \ge V_{cc} - 0.2\text{V}$		sale 2 le f	50	μA
Output low Voltage	Vol	IoL = 2.1mA	-	Telfs W	0.4	V-L
Output High Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.4	-	Toblish	V

Notes: 1) Typical limits are at V_{cc} =5.0V, Ta=+25°C 2) *: V_{LLmn} =-0.3V

ECAPACITANCE ($Ta=25^{\circ}\text{C}$, f=1.0MHz)

Item	Symbol	Test Conditions	typ	adiaW max	Unit
Input Capacitance	CIN	$V_{IN} = 0 \text{ V}$	3	5	pF
Input/Output Capacitance	Ciro	V _{1.0} =0V	5	2 20 47 - 224	pF

Note: 1) This parameter is sampled and not 100% tested.

BAC CHARACTERISTICS ($Ta=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{cc}=5\text{V}\pm10\%$ unless otherwise noted)

• AC TEST CONDITIONS

Output Load 1 TTL Gate and CL = 100pF (Including Scope & Jig)

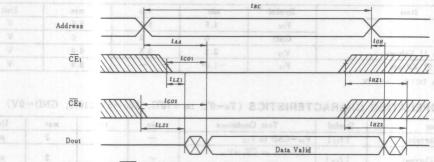
• READ CYCLE

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Item	Symbol	HM6117LFP-3		HM6117LFP-4		17.74
Item		min	max	min	max	Unit
Read Cycle Time	trc	150	_	200	-	ns
Address Access Time	tan	_	150	- 11	200	ns
Chip Enable (\overline{CE}_1) to Output	tcoi	_	150	-	200	ns
Chip Enable (CE2) to Output	tcoz	100 b	150	4 STRIZZO 5	200	ns
Chip Enable (CE1) to Output in Low Z	tuzi	10	30W_UNA	10	STYLETCI_	ns
Chip Enable (\overline{CE}_2) to Output in Low Z	tLZ2	10	deducer often	10		ns
Chip Disable (CE1) to Output in High Z	tHZ1	0	70	aggn 0 o a	80	ns
Chip Disable (CE2) to Output in High Z	tHZ2	0	70	0	80	ns
Output Hold from Address Change	toн	15	ut non	15	531-54	ns

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● TIMING WAVEFORM OF READ CYCLE (Notes 1) TIGHOO DANTAREAD DO GEGRENMODERS

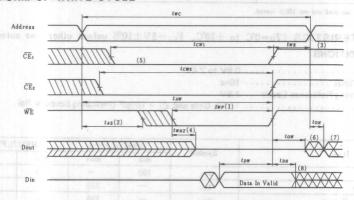


NOTES: 1. WE is High for Read Cycle.

• WRITE CYCLE

Ass 03 Item	Sund at 1	HM6117LFP-3		HM6117LFP-4		Unit	
Item	Symbol.	min	max	min	max	Unit	
Write Cycle Time	twc	150	35 -	200	ाक्टकड स	ns	
Chip Enable (CE1) to End of Write	tewn	100	Cary - 125-	120	- 30	ns	
Chip Enable (CE2) to End of Write	tcw2	110	and -	130	er Sa ga ly	ns	
Address Set Up Time	tas	20		20	- 50	ns ns	
Address Valid to End of Write	tAW	130	Level - 10	150	- agustia	ns	
Write Pulse Width	twp	100	task - sel	120	Voitage	ns	
Write Recovery Time	twr	15	7/85+-	15	line and Theoline	ns	
Write to Output in High Z	twnz	0	60	0	70	ns	
Data to Write Time Overlap	tow	50	_	60	-	ns	
Data Hold from Write Time	t _{DH}	20	2H2007] = [20	HOMAT	ns	
Output Active from End of Write	anotitow Dues T	10	8 -	10	ctul =	ns	

TIMING WAVEFORM OF WRITE CYCLE



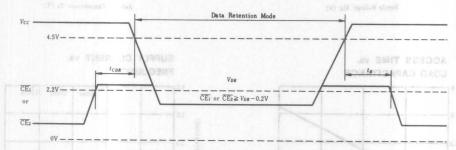
- NOTES: 1 A write occurs during the overlap $(t_W p)$ of low \overline{CE}_1 , \overline{CE}_2 and \overline{WE} .
 - t_{AS} is measured from the address changes to the biginning of the write.
 - t_{WR} is measured from the earlier of CE₁, CE₂ or WE going high to the end/of write cycle.
- During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 5. If the \overline{CE}_1 or \overline{CE}_2 low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transitions, output remain in a high im-
- pedance state.
- 6. Dout is the same phase of write data of this write cycle.
- Dout is the read data of next address.
- If CE₁ and CE₂ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°Cto +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
V _{CC} for Data Retention	V_{DR1}	$\overline{\text{CE}}_1 \ge V_{cc} - 0.2\text{V},$ $V_{IN} \ge V_{cc} - 0.2\text{V} \text{ or } V_{IN} \le 0.2\text{V}$	2.0	_	-	V
Vcc for Data Retention	V _{DR2}	$\overline{CE}_2 \ge V_{cc} - 0.2V$	2.0	_	- 1	V
Data Retention Current	ICCDRI	$V_{CC} = 3.0 \text{V}, \overline{\text{CE}}_1 \ge 2.8 \text{V},$ $V_{IN} \ge 2.8 \text{V} \text{ or } V_{IN} \le 0.2 \text{V}$	-	-	30*	μА
Data Retention Current	ICCDR2	$V_{cc}=3.0V$, $\overline{\text{CE}}_2 \ge V_{cc}-0.2V$	- T. C.	-	30*	μА
Chip Deselect to Data Retention Time	tcor	See Retention Waveform	0		-	ns
Operation Recovery Time	t _R	See Retention Waveform	t _{RC} **	-	-160	ns

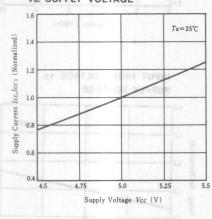
^{* 10} µA max at Ta=0°C to +40°C, V_{IL} min=-0.3V

● LOW Vcc DATA RETENTION WAVEFORM

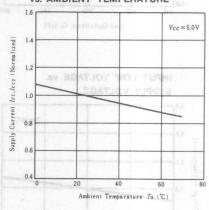


NOTE: 1. \overline{CE}_2 controls Address buffer, \overline{WE} buffer, \overline{CE}_1 buffer and D_{IN} buffer. If \overline{CE}_2 controls data retention mode, V_{IN} level (address, \overline{WE} , \overline{CE}_1 , $D_{I/O}$) can be in the high impedance state. If \overline{CE}_1 controls data retention mode, V_{IN} level (address, \overline{WE} , \overline{CE}_2 , $D_{I/O}$) must be $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$.

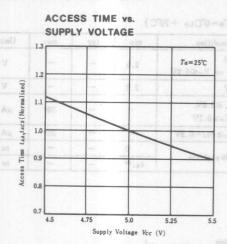
SUPPLY CURRENT vs. SUPPLY VOLTAGE

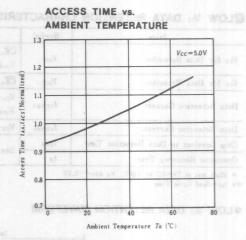


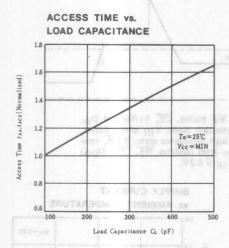
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

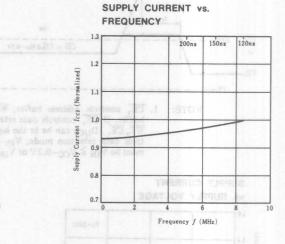


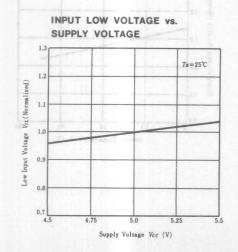
^{**} tRC - Read Cycle Time

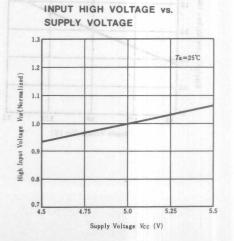




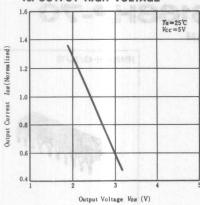




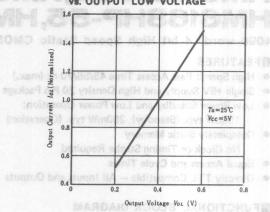




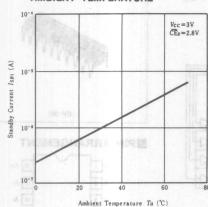
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



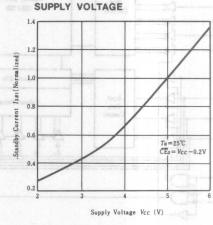
OUTPUT LOW CURRENT VS. OUTPUT LOW VOLTAGE



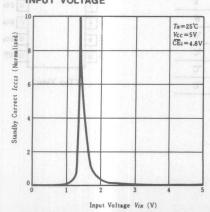
STAND-BY CURRENT VS. AMBIENT TEMPERATURE



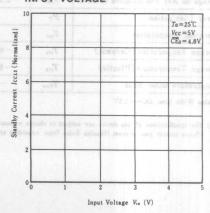
STAND-BY CURRENT VS.



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE





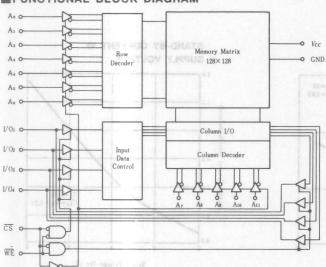
HM6168H-45,HM6168H-55, Under Development HM6168H-70,HM6168HP-4 HM6168HP-55.HM6168HP-70

4096-word×4-bit High Speed Static CMOS RAM

FEATURES

- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation; 100µW typ. (Standby), 250mW typ. (Operation)
- Completely Static Memory No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible All Inputs and Outputs

FUNCTIONAL BLOCK DIAGRAM

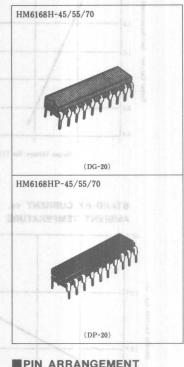


MADSOLUTE MAXIMUM RATINGS

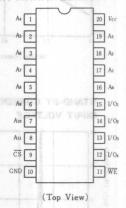
Item The The	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	VIN	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature (Ceramic)	Tats	-65 to +150	°C
Storage Temperature (Plastic)	Tsts	-55 to +125	°C
Temperature under Bias	Thine	-10 to +85	°C

* Pulse Width 20ns, DC = -0.5V

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales Dept. reqarding specifications.



PIN ARRANGEMENT

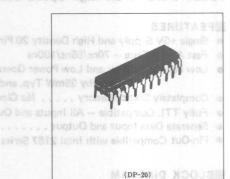


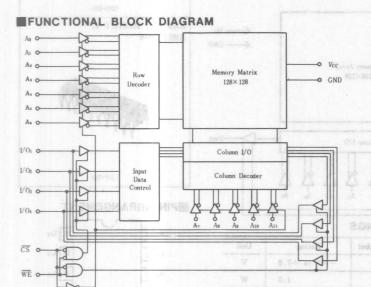
HM6168HLP-45, HM6168HLP-55, HM6168HLP-70 Under Development

4096-word×4-bit High Speed Static CMOS RAM to boog April 11d-1 x bic w-1880

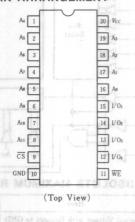
FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
 5µW typ. (Standby), 250mW typ. (Operation)
- Completely Static Memory
 No Clock or Timing Strobe Required
- Equal Access and Cycle Times.
- Directly TTL Compatible All Inputs and Outputs
- Capable of Battery back up Operation





PIN ARRANGEMENT



MADSOLUTE MAXIMUM RATINGS

en at Item	Symbol	Rating	Unit	Storage Temperators (Ceramic). To
Voltage on Any Pin Relative to GND	V_{IN}	-3.5* to +7.0	V	
Power Dissipation	P_T	1.0	W	
Operating Temperature	Topr	0 to +70	°C	BRECOMMENCED DC OPERATING
Storage Temperature	T_{stg}	-55 to +125	°C	(0°C≤Tu≤70°C)
Temperature under Bias	Thias	-10 to +85	°C	nies Joseph State Company

* Pulse Width 20ns, DC=-0.5V

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications

OHITACHI

HM6167,HM6167-6,HM6167-8, HM6167P,HM6167P-6,HM6167P-8

16384-word×1-bit High Speed Static CMOS RAM

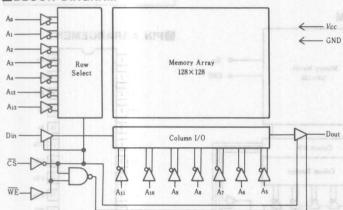
FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation

Stand-by 25mW Typ, and Operating 150mW Typ.

- Completely Static Memory No Clock nor Refresh Required
- Fully TTL Compatible All Inputs and Output
- Separate Data Input and Output Three State Output
- Pin-Out Compatible with Intel 2167 Series

BLOCK DIAGRAM



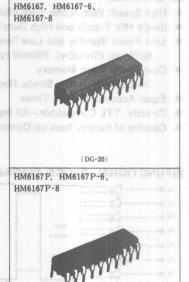
MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	-0.5 to $+7.0$	V
Power Dissipation	PT	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature(Plastic)	Tets	-55 to +125	°C
Storage Temperature(Ceramic)	Tets	-65 to +150	°C

■RECOMMENDED DC OPERATING CONDITIONS

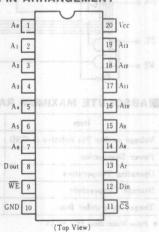
 $(0^{\circ}C \leq Ta \leq 70^{\circ}C)$

Item	Symbol	min	typ	max	Unit
S	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High Voltage	VIH	2.2	_	6.0	V
Input Low Voltage	VIL	-0.5	-	0.8	V



PIN ARRANGEMENT

(DP-20)



TRUTH TABLE

CS	WE	Mode	Vcc Current	Output Pin	Reference Cycle
Н	×	Not Selected	I _{SB} , I _{SB1}	High Z	
L	Н	Read	Icc	Dout	Read Cycle 1, 2
L	L	Write	Icc dd	High Z	Write Cycle 1, 2

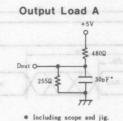
DC AND OPERATING CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $T_a=0\%$ to +70%)

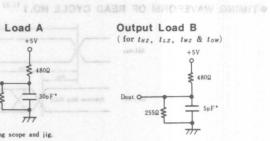
Item	Symbol	Test Conditions	475	min	typ	max	Unit
Input Leakage Current	ILI	$V_{CC} = 5.5 \text{V}, V_{IN} = 0 \text{V} \sim V_{CC}$	59		- 1	2	μA
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{OUT} = 0 \text{ V} \sim V_{CC}$	75		12 <u>17</u> /7 (2	μΑ
Operating Power Supply Current	Icc	$\overline{\text{CS}} = V_{IL}$, Output Open	Yell	_	30	60	mA
P-5 66 00	IsB	$\overline{\text{CS}} = V_{IH}$	2.00		5	20	mA
Standby Power Supply Current	I_{SB1}	$\overline{CS} = V_{CC} - 0.2V$ $V_{IN} \le 0.2V \text{ or } \ge V_{CC} - 0.2V$	dgid tanti	nt W die d biografia	0.02	2 2 S	mA _{stel}
Output Low Voltage	Vol	$I_{OL} = 8 \mathrm{mA}$	thus.	to most Vest (60) Just 100%	da sampled i	0.4	V
Output High Voltage	V _{OH}	$I_{OH} = -4 \mathrm{mA}$		2.4	-	_	V

Note) Typical limits are at V_{cc} =5.0V, Ta=25°C and specified loading.

MAC TEST CONDITIONS

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure





THEM WAVEFORM OF READ CYCLE NO. 2 11.11

ECAPACITANCE ($Ta=25^{\circ}C$, f=1.0 MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	CIN	5	pF	$V_{IN} = 0 \text{ V}$
Output Capacitance	Соит	6	pF	$V_{OUT} = 0 \text{ V}$

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = 0^{\circ}C$ to $70^{\circ}C$, unless otherwise noted.) •READ CYCLE

T	C 1.1	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	trc	70	or boing	85	Afficanti di	100	- 1	ns
Address Access Time	taa	_	70	-	85	-	100	ns
Chip Select Access Time	tacs	_	70	-	85		100	ns
Output Hold from Address Change	t _{OH}	5	_	5	-	5	- 4	ns
Chip Selection to Output in Low Z	tLZ	5	-	5	_	5		ns
Chip Deselection to Output in High Z	tHZ	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	tpu	0	-	0	_	0	- 1	ns
Chip Deselection to Power Down Time	tpD	_	35	-	40	111-	45	ns

• WRITE CYCLE

oloco eser Item	Symbol	HM6167,	HM6167P	HM6167-6,	HM6167-6, HM6167P-6 HM6167-8, HM6167P-8			Unit	Notes
rtem X	Symbol	min	max	min	max	min	max	Unit	Notes
Write Cycle Time	twc	70	Tee	85	- bno S	100		ns	2
Chip Selection to End of Write	t cw	55	-T	65	- asiaV	80		ns	
Address Valid to End of Write	t _{AW}	55	-	65	-	80		ns	
Address Setup Time	tas	%010 V	- H) 8	0 0	RACTE	MOO DE	DIANES	ns	MDC A
Write Pulse Width	twp	40	est Conda	45	[[primar)	55		ns	
Write Recovery Time	twR	0	-v6-,v	0	Tail	0	1000	ns	la I messi
Data Valid to End of Write	t _{DW}	30	- 4 0	35	5 Tool	40		ns	L towns
Data Hold Time	t _{DH}	0	plest. Coes	0	5 - 1	0	Supply Cut	ns	edizersin0
Write Enable to Output in High Z	twz	0	30	0	40	0	40	ns	3, 4
Output Active from End of Write	tow	0	-170	.0	-	0		ns	3,4

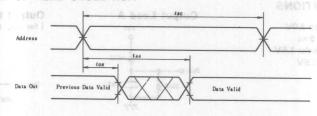
Notes) 1. If $\overline{\text{CS}}$ goes high simultaneouly with $\overline{\text{WE}}$ high, the output remains in a high impedance state.

2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.

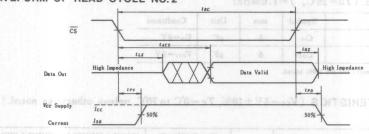
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

4. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF READ CYCLE NO.1 1), 2)



TIMING WAVEFORM OF READ CYCLE NO. 2 1), 3)

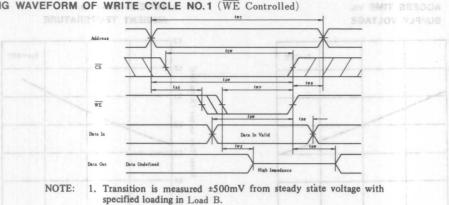


NOTES: 1. WE is high and CS is low for READ cycle.

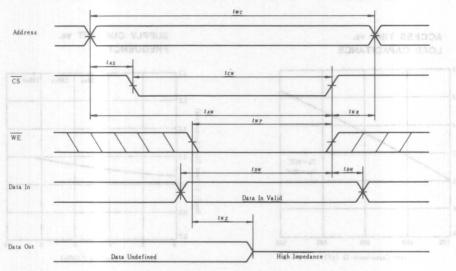
2. Addresses valid prior to or coincident with CS transition low.

 Transition is measured ±500 mV from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE Controlled)

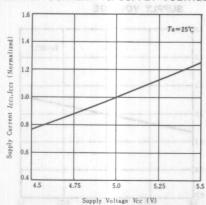


TIMING WAVEFORM OF WRITE CYCLE No. 2 (CS Controlled)

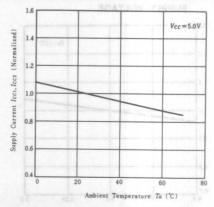


Note) Transition is measured $\pm 500 \, \text{mV}$ from steady state voltage with specified loading in Load B.

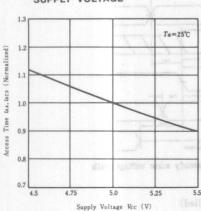
SUPPLY CURRENT vs. SUPPLY VOLTAGE



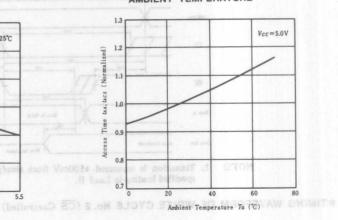
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



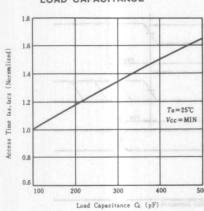
ACCESS TIME vs.



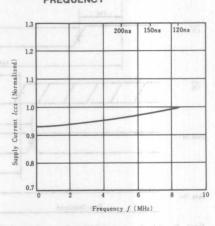
(bellostro) 200 F.O. B. ACCESS TIME vs. VAC-ESVAW DAIMIT &



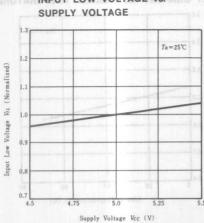
ACCESS TIME vs.



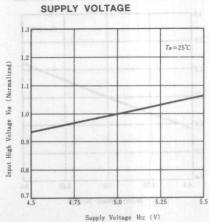
SUPPLY CURRENT vs. FREQUENCY



CURRY VOLTAGE VS. 110 Y 19412

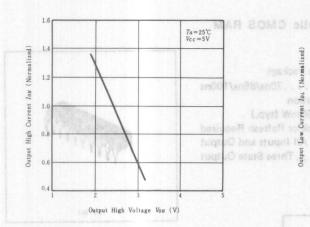


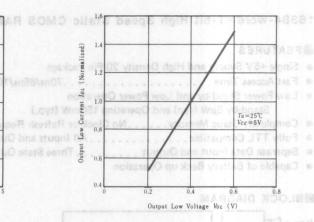
SUPPLY VOLTAGE VS.





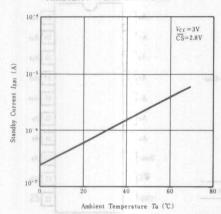
OUTPUT LOW CURRENT vs.
OUTPUT LOW VOLTAGE

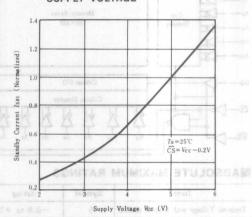




STANDBY CURRENT vs. AMBIENT TEMPERATURE

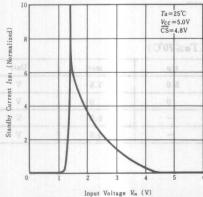
STANDBY CURRENT vs. SUPPLY VOLTAGE

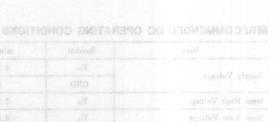




STANDBY CURRENT vs.

INPUT VOLTAGE



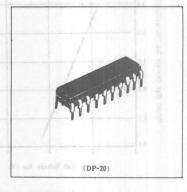


HM6167LP, HM6167LP-6, HM6167LP-8

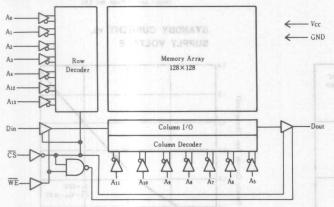
16384-word×1-bit High Speed Static CMOS RAM

FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Low Power Stand-by and Low Power Operation
 Stand-by 5μW (typ) and Operating 150mW (typ.)
- Completely Static Memory. No Clock or Refresh Required
- Fully TTL Compatible All Inputs and Output
- Separate Data Input and Output Three State Output
- Capable of Battery Back up Operation



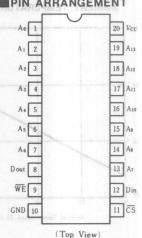
BLOCK DIAGRAM



MABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tate	-55 to +125	°C

PIN ARRANGEMENT



RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}C \le Ta \le 70^{\circ}C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High Voltage	VIH	2.2		6.0	V
Input Low Voltage	VIL	-0.5	- 1	0.8	V

OTIMING WAVE ORM OF READ CYCLE NO.1 11.2

TRUTH TABLE

CS	WE	Mode	Vcc Current	Output Pin	Reference Cycle
Н	×	Not Selected	I_{SB} , I_{SB1}	High Z	
L	Н	Read	Icc	Dout	Read Cycle 1, 2
L	L -	Write	Icc	High Z	Write Cycle 1, 2

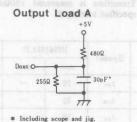
DC AND OPERATING CHARACTERISTICS ($V_{cc} = 5 \text{V} \pm 10\%$, $Ta = 0 \sim +70^{\circ}\text{C}$)

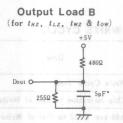
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	$V_{CC}=5.5 \text{ V}$ $V_{IN}=0 \text{ V} \sim V_{CC}$		_	2	μΑ
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}$, $V_{out} = 0 \text{ V} \sim V_{CC}$	25_	_	2	μΑ
Operating Power Supply Current	Icc	$\overline{\text{CS}} = V_{IL}$, Output Open	_	30	60	mA
Mary Propins	IsB	$\overline{\mathrm{CS}} = V_{IH}$	-	5	20	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} = V_{cc} - 0.2 \text{V}$ $V_{IN} \le 0.2 \text{V or } \ge V_{cc} - 0.2 \text{V}$	- 10 40	1	50	μА
Output Low Voltage	Vol	$I_{OL} = 8 \mathrm{mA}$	19922 34	-	0.4	V
Output High Voltage	Von	$I_{OH} = -4 \mathrm{mA}$	2.4	-	_	V

Note) Typical limits are at $V_{cc}=5.0$ V, Ta=25°C and specified loading.

MAC TEST CONDITIONS

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure





EXAMPLE 1.0 CAPACITANCE $(Ta=25^{\circ}\text{C}, f=1.0\text{MHz})$

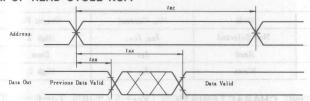
Item	Symbol	max	Unit	Conditions
Input Capacitance	CIN	5	pF	$V_{IN} = 0 \text{ V}$
Output Capacitance	Соит	6	pF	$V_{OUT} = 0 \text{ V}$

Note) This parameter is sampled and not 100% tested.

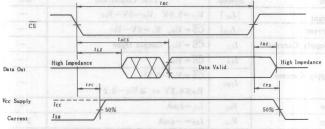
■AC CHARACTERISTICS ($Ta=0^{\circ}$ C to $+70^{\circ}$ C, Vcc=5V $\pm10\%$, unless otherwise noted.) • READ CYCLE

Item	C 1 1	HM6	167LP	HM61	67LP-6	HM6167LP-8		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	tRC	70		85	_	100	_	ns
Address Access Time	taa	_	70	X	85	160	100	ns
Chip Select Access Time	tacs		70	+ 1	85	-	100	ns
Output Hold from Address Change	t _{OH}	5	-	5	1-	5	_	ns
Chip Selection to Output in Low Z	tLZ	5		5	-	5	-	ns
Chip Deselection to Output in High Z	tHZ	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	tpu	0	/ -	0		0	-	ns
Chip Deselection to Power Down Time	tpD	4	35	_	40	-	45	ns

TIMING WAVEFORM OF READ CYCLE NO.1 1), 2)



TIMING WAVEFORM OF READ CYCLE NO. 2 1,3)



NOTES: 1. WE is high and CS is low for READ Cycle.

- 2. Addresses valid prior to or coincident with $\overline{\text{CS}}$ transition low.
- 3. Transition is measured ±500mV from steady state voltage with specified loading B.

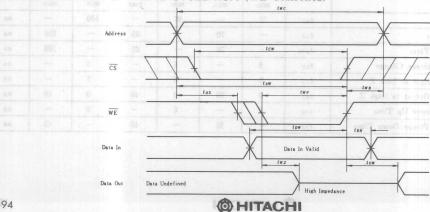
• WRITE CYCLE

Item	Symbol	HMe	5167LP	HM616	7LP-6	HM61	67LP-8	Unit	Notes
item	Symbol	min	max	min	max	min	max	ata ibes	Notes
Write Cycle Time	twc	70	tites	85	-	100	_	ns	2
Chip Selection to End of Write	tcw	55	-	65	-	80	- 1	ns	
Address Valid to End of Write	t _{AW}	55	albilett s	65		80	_	ns	
Address Setup Time	tas	0	-	0	-	0	-	ns	
Write Pulse Width	twp	40	-	45	M0.1-1	55	T. TION	ns	HADE
Write Recovery Time	tw _R	0	of filters O	0	Kee	0	2	ns	
Data Valid to End of Write	t _{DW}	30	7/0	35	H-Ta	40	- 1	ns	Input Ca
Data Hold Time	t _{DH}	0	70-	0 1	- a	0	-	ns	Dames O
Write Enable to Output in High Z	twz	0	30	0	40	0	40	ns	3,4
Output Active from End of Write	tow	0	-	0	-	0	_	ns	3,4

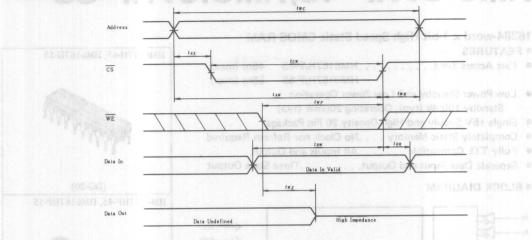
Notes) 1. If $\overline{\text{CS}}$ goes high simultaneouly with $\overline{\text{WE}}$ high, the output remains in a high impedance state.

- 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
- 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
- $4\,.$ This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE No. 2 (CS Controlled)

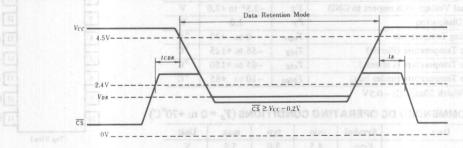


■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	O'Al moule	2.0	1	- 1	V
Data Retention Current	,	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{ V}$	+	11-	20*	1.
	ICCDR	$V_{in} \ge V_{CC} - 0.2 \mathrm{V}$ or	八光	13-1	30**	μΑ
Chip Deselect to Data Retention Time	tcor	$0 \mathrm{V} \! \leq \! V_{in} \! \leq \! 0.2 \mathrm{V}$	0	11.5	- 1	ns
Operation Recovery Time	t_R		tRC△	market of	_	ns

 \triangle t_{RC} - Read Cycle Time

LOW Vcc DATA RETENTION WAVEFORM



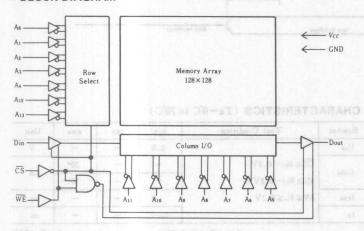
HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

16384-word x 1-bit High Speed Static CMOS RAM

FEATURES

- Low Power Standby and Low Power Operation Standby 100μW (typ), Operating 200mW (typ)
- Single +5V Supply and High Density 20 Pin Package
- · Completely Static Memory No Clock nor Refresh Required
- Fully TTL Compatible All Inputs and Output
- Separate Data Input and Output. Three State Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

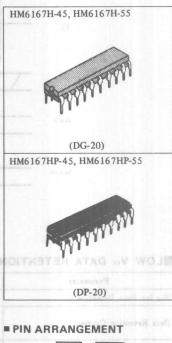
Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature (Plastic)	Tstg	-55 to +125	°C
Storage Temperature (Ceramic)	Tstg	-65 to +150	°C
Storage Temperature (under bias)	Thias	-10 to +85	°C

^{*} Pulse Width 20ns, DC: -0.5V

■ RECOMMENDED DC OPERATING CONDITIONS $(T_a = 0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	min	typ	max	Unit
Complex Welders	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Y X7-14	VIH	2.2	-	6.0	V
Input Voltage	VIL	-3.0*	_	0.8	V

^{*} Pulse Width: 20ns, DC: V_{IL} (min) = -0.5V





MAC CHARACTERISTICS (Vec-5V±10%, Ta=0°C to 70°C, paless oil wise no BAC HTURT =

CS	WE	Mode	Vcc Current	Dout Pin	Ref. Cycle
Н	×	Not selected	ISB, ISB1	High-Z	
L	Н	Read	Icc also	Dout	Read Cycle
L	as L	Write	Icc 28	High-Z	Write Cycle

■DC AND OPERATING CHARACTERISTICS (V_{cc}=5V±10%, T_a=0℃ to +70℃)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	$V_{CC} = 5.5 \text{V}, V_{IN} = 0 \text{V} \sim V_{CC}$	- 2 M	6.1 ml_047	2	μA
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{OUT} = 0 \text{ V} \sim V_{CC}$	2 1981	East Surge St.	2	μΑ
Operating Power Supply Current	Icc	$\overline{\mathrm{CS}} = V_{IL}$, Output Open	_	40	80	mA
	IsB	$\overline{\mathrm{CS}} = V_{IH}$	-	10	20	mA
Standby Power Supply Current	Isaı	$\overline{CS} \ge V_{cc} - 0.2 V$ $V_{lN} \le 0.2 V \text{ or } \ge V_{cc} - 0.2 V$	unally use ester nperasuse and evice.	0.02	2	mA
Output Low Voltage	Vol	$I_{OL} = 8 \mathrm{mA}$	EAD cyco.	ref Culi	0.4	V
Output High Voltage	Von	$I_{OH} = -4 \mathrm{mA}$	2.4	entras er	5. Denice	V

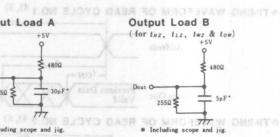
Note) Typical limits are at Vcc=5.0V, Ta=25°C and specified loading.

MAC TEST CONDITIONS

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure

Output Load A +5V ≸ 480Ω Dout O-2550 €

* Including scope and jig.



ECAPACITANCE ($Ta=25^{\circ}C$, f=1.0 MHz)

Item Schabour	Symbol	typ	max	Unit	Conditions
Input Capacitance	CIN	3	5	pF	V _{IN} = 0 V
Output Capacitance	Соит	5	7	pF	$V_{OUT} = 0 \text{ V}$

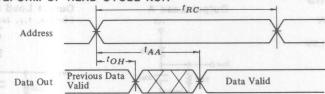
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Vcc=5V±10%, Ta=0°C to 70°C, unless otherwise noted.) •READ CYCLE

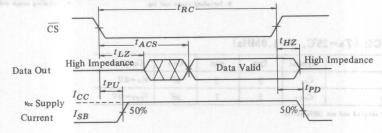
Symbol	HM6167H/P-45		HM6167HP-55		Unia	Notes
Symbol	min	max	min	max	Unit	Notes
tRC	45		55		ns	(1)
tAA	- 3	45	-	55	ns	
tACS	EVE-SIV)	45	BTDARK	55	ns	BOC AND
toH	5	eT -	5	_	ns	
tLZ	5	9 97 3 4	5		ns	(2) (3) (7)
tHZ	0	30	0	30	ns	(2)(3)(7)
tPU	0		0	-	ns	
tPD	susper to	30	2 591	30	ns	e 1 -3811428453
	Symbol tRC tAA tACS tOH tLZ tHZ	Symbol min	min max tRC 45 - tAA - 45 tACS - 45 tOH 5 - tLZ 5 - tHZ 0 30 tPU 0 -	min max min tRC 45 - 55 tAA - 45 - tACS - 45 - tOH 5 - 5 tLZ 5 - 5 tHZ 0 30 0 tPU 0 - 0	Symbol min max min max tRC 45 - 55 - tAA - 45 - 55 tACS - 45 - 55 tOH 5 - 5 - tLZ 5 - 5 - tHZ 0 30 0 30 tPU 0 - 0 -	Symbol min max min max Unit tRC 45 - 55 - ns tAA - 45 - 55 ns tACS - 45 - 55 ns tOH 5 - 5 - ns tLZ 5 - 5 - ns tHZ 0 30 0 30 ns tPU 0 - 0 - ns

- NOTES: 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
 - 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 - 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
 - 4. WE is High for READ cycle.
 - 5. Device is continuously selected, $\overline{CS} = V_{IL}$.
 - 6. Addresses valid prior to or coincident with $\overline{\text{CS}}$ transition low.
 - 7. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF READ CYCLE NO.1 4), 5)



TIMING WAVEFORM OF READ CYCLE NO.2 4), 6)



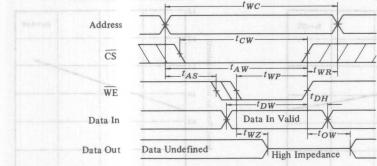
• WRITE CYCLE

	UMC16	7U/D 45	UMC167	II/D cc		
Symbol	пмото/Н/Р-43		HM010/	HM616/H/F-33		Notes
	min	max	min	max		
twc	45	-	55		ns	(2)
tcw	40	-	50	-	ns	
tAW	40		50	-	ns	11.5
tAS	0	-	0	11-	ns	
tWP	25	-	35		ns	di g
twR	0	-	0		ns	li a
tDW	25		25	-	ns	1
tDH	0	-	0	M	ns	1 3
twz	0	25	0	25	ns	(3) (4)
tow	0	-1	0		ns	(3) (4)
	tCW tAW tAS tWP tWR tDW tDH	min min	min max tWC 45 tCW 40 tAW 40 tAS 0 tWP 25 tWR 0 tDW 25 tDH 0 tWZ 0 25 -	Symbol min max min tWC 45 - 55 tCW 40 - 50 tAW 40 - 50 tAS 0 - 0 tWP 25 - 35 tWR 0 - 0 tDW 25 - 25 tDH 0 - 0 tWZ 0 25 0	Symbol min max min max tWC 45 - 55 - tCW 40 - 50 - tAW 40 - 50 - tAS 0 - 0 - tWP 25 - 35 - tWR 0 - 0 - tDW 25 - 25 - tDH 0 - 0 - tWZ 0 25 0 25	Symbol min max min max twc 45 - 55 - ns tcw 40 - 50 - ns tAw 40 - 50 - ns tAs 0 - 0 - ns twp 25 - 35 - ns twr 0 - 0 - ns tDW 25 - 25 - ns tDH 0 - 0 - ns twz 0 25 0 25 ns

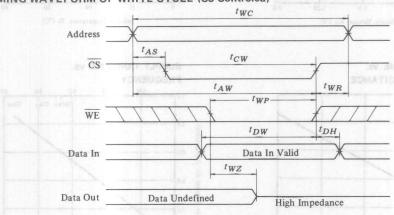
NOTES: 1. If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance states.

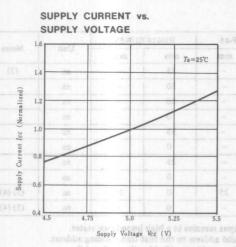
- All write cycle timings are referenced from the last valid address to the first transitioning address.
 Transition is measured ±500mV from steady state voltage with specified loading in Load B.
- 4. This parameter is sampled and not 100% tested.

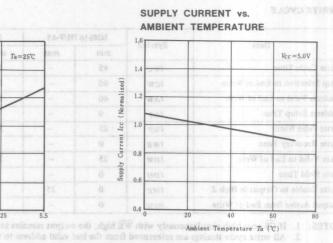
TIMING WAVEFORM OF WRITE CYCLE (WE Controled)

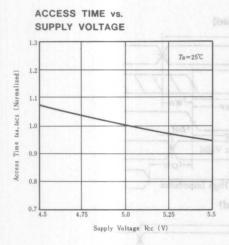


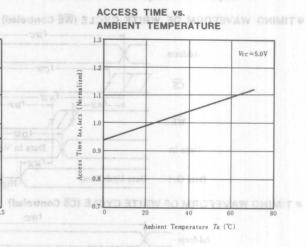
• TIMING WAVEFORM OF WRITE CYCLE (CS Controled)

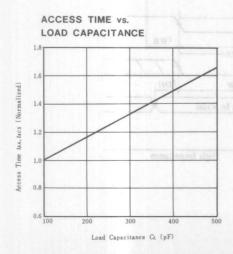


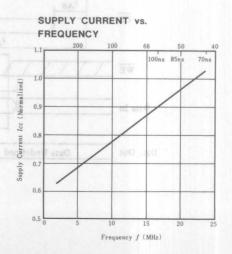




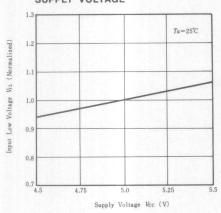




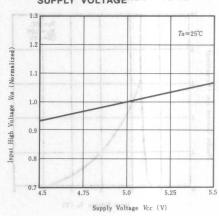




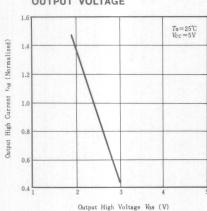
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



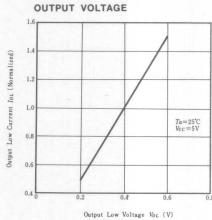
INPUT HIGH VOLTAGE vs.
SUPPLY VOLTAGE



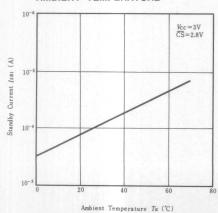
OUTPUT CURRENT vs.
OUTPUT VOLTAGE



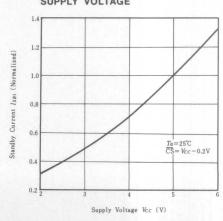
OUTPUT CURRENT vs.



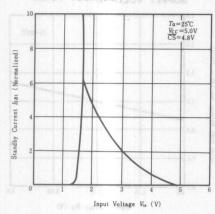
STANDBY CURRENT vs.
AMBIENT TEMPERATURE

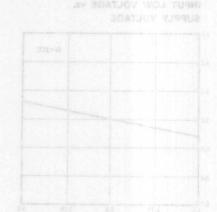


STANDBY CURRENT vs. SUPPLY VOLTAGE

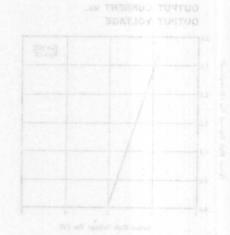


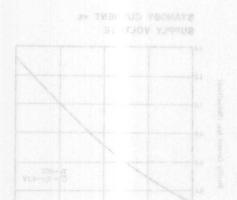














HM6167HCG-45,HM6167HCG-55

16384-word×1-bit High Speed Static CMOS RAM

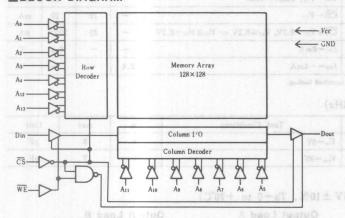
FEATURES

- High Density 20 pin Leadless Chip Carrier
- High Speed: Fast Access Time 45/55ns Max.
- Low Power Standby and Low Power Operation Standby: 100μW typ., Operation: 200mW typ.

No Clock or Timing Strobe Required

- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Output

■BLOCK DIAGRAM



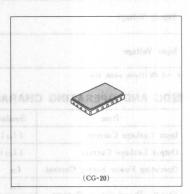
MADE ADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	T_{sig}	-65 to +150	°C
Temperature Under Bias	Thias	-10 to +85	°C

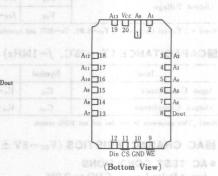
^{*} with respect to GND.

TRUTH TABLE

CS	WE	Mode	Vcc Current	Dout Pin	Ref. Cycle
Н	×	Not selected	I_{SB} , I_{SB1}	High-Z	and another the
L	Н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc	High-Z	Write Cycle



PIN ARRANGEMENT



Vo.1 talevel constant

 $V_{IN} \min = -3.5 \text{V (Pulse width 20ns)}$

TRECOMMENDED DC OPERATING CONDITIONS $(Ta=0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	OMOminitest	typ?	M max X	TOW Unit
	V_{cc}	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
	V_{IH}	2.2	dless Onip Car	6.0	V
Input Voltage	V_{IL}	-0.5*	ande\de simil	0.8	V

^{* -3.0}V (Pulse width 20ns)

DC AND OPERATING CHARACTERISTICS $(V_{cc}=5V\pm10\%, T_a=0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	I _{LI}	V_{CC} =5.5V, V_{IN} =0V to V_{CC}	liditson	10.5 II	2	μΑ
Output Leakage Current	I _{LO}	$\overline{\text{CS}} = V_{IH}, \ V_{OUT} = 0V \text{ to } V_{CC}$	-	-	2	μΑ
Operating Power Supply Current	I_{cc}	$\overline{\mathrm{CS}} = V_{IL}$, Output Open	_86a	40	80	mA
0,00	I_{SB}	$\overline{\mathrm{CS}} = V_{IH}$	-	10	20	mA
Standby Power Supply Current	I_{SB1}	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}, \ V_{IN} \le 0.2 \text{V} \text{ or } V_{IN} \ge V_{CC} - 0.2 \text{V}$	-	20	2000	μΑ
I PARAMOENENT	Vol	$I_{OL} = 8 \mathrm{mA}$	-	-	0.4	V
Output Voltage	V_{OH}	$I_{OH} = -4 \mathrm{mA}$	2.4	-	15	V

Note) * : Typical limits are at $V_{cc}=5.0$ V, Ta=25°C and specified loading.

EXAMPLE 1 CAPACITANCE $(Ta=25^{\circ}\text{C}, f=1\text{MHz})$

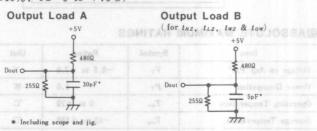
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0$ V	3	5	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}$	5	7	pF

Note) This parameter is sampled and not 100% tested.

EAC CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = 0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: GND to 3.0V Input Rise and Fall Times: 5 ns Output Reference Levels: 1.5V



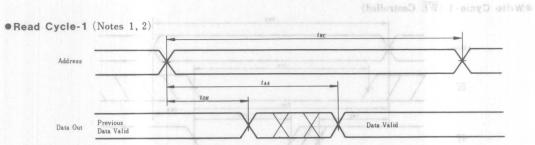
• READ CYCLE

	0 1 1	HM6167H	ICG-45	HM6167H	HM6167HCG-55		Natara
Item	Symbol	min	max	min	max	Unit	Notes
Read Cycle Time	trc	45		55		ns	1
Address Access Time	taa	Jastrol7 s.V	45	900M	55	ns	SO
Chip Select Access Time	tacs	iss, iss	45	Datasias It	55	ns	THE R
Output Hold from Address Change	toH	5		5	-	ns	
Chip Selection to Output in Low Z	tLZ	5		5		ns	2, 3, 4
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 4
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	ns	
Chip Deselection to Power Down Time	tpD	-	30	_	30	ns	

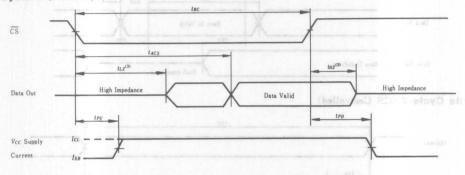
Notes) 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.

At any given temperature and voltage condition, t_{RZ} max is less than t_{LZ} min both for a given device and from device to device.
 Transition is measured ±500mV from steady state voltage with specified loading in Load B.

Transition is measured ±500mV from steady state
 This parameter is sampled and not 100% tested.



• Read Cycle-2 (Notes 1, 3)



Notes) 1. WE is high for Read Cycle.

2. Address valid prior to or coincident with $\overline{\text{CS}}$ transition low.

3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

• WRITE CYCLE

1.2	C1	HM616	57HCG-45	HM6167	HCG-55	Unit	Notes
Item	Symbol	min	max	min	max	Unit	Notes
Write Cycle Time	twc	45	- 1	55	-	ns	2
Chip Selection to End of Write	tcw	40		50		ns	d well
Address Valid to End of Write	t _{AW}	40		50	_	ns	
Address Setup Time	tas	0	(4)	. 0	_	ns	
Write Pulse Width	twp	25	_	35	-	ns	
Write Recovery Time	t _{WR}	0	_	0	a	ns	01:00
Data Valid to End of Write	t _{DW}	25	-	25	_	ns	
Data Hold Time	t _{DH}	0	-	0	-	ns	
Write Enable to Output in High Z	tw2	0	25	0	25	ns	3,4
Output Active from End of Write	tow	0	-	0	_	ns	3, 4

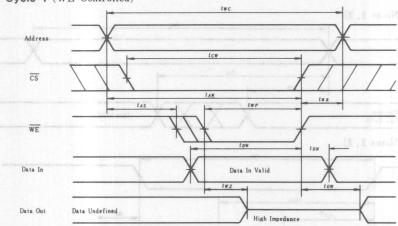
Notes) 1. If \overline{CS} goes high simultaneouly with \overline{WE} high, the output remains in a high impedance state.

2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.

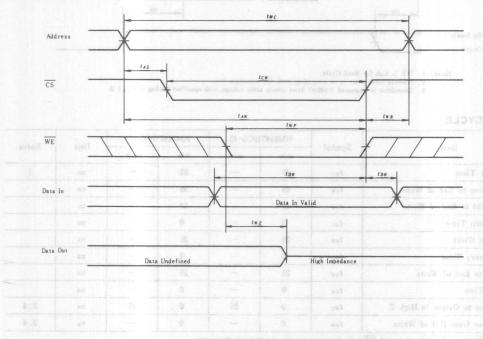
3. Transition is measured $\pm 500 \text{mV}$ from steady state voltage with specified loading in Load B.

4. This parameter is sampled and not 100% tested.

• Write Cycle-1 (WE Controlled)



• Write Cycle-2 (CS Controlled)

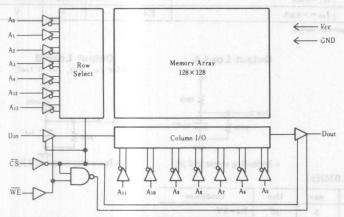


HM6167HLP-45, HM6167HLP-55

16384-word x 1-bit High Speed Static CMOS RAM

- FEATURES
- Low Power Standby and Low Power Operation
 Standby 5μW (typ) and Operating 200mW (typ)
- Capable of Battery Back-up Operation
- Single +5V Supply and High Density 20 Pin Package
- Completely static Memory
 No Cleak or Timing Strake
 - No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible All Inputs and Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

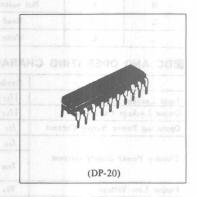
Item	Symbol	Rating	Unit	Serest of	1911 men fina or una property and financial
Terminal Voltage with respect to GND	V_T	-3.5* to +7.0	V		(Top View)
Power Dissipation	P_T	1.0	W	Trans	
Operating Temperature	Topr	0 to +70	°C		
Storage Temperature	Tstg	-55 to +125	°C		
Storage Temperature Under Bias	Thias	-10 to +85	°C		

* Pulse Width 20ns, DC: -0.5V

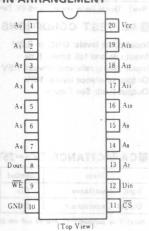
■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \text{ to } +70^{\circ}\text{C}$)

Item	Symbol	min	typ	max	Unit
Committee Walters	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Tarana Waltara	VIH	2.2	_	6.0	V
Input Voltage	V_{IL}	-3.0*	_trc	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = -0.5V



PIN ARRANGEMENT



TRUTH TABLE

CS	WE	Mode	Vcc Current	Dout Pin	Ref. Cycle
Н	×	Not selected	IsB, IsB1	High-Z	in the brown ARER
L	Н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc - GANTA	High-Z	Write Cycle

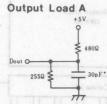
DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, Ta=0~+70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	$V_{cc}=5.5 \text{ V}$ $V_{IN}=0 \text{ V} \sim V_{cc}$	sedn an-s	198 2(9)	2	μA
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}$, $V_{out} = 0 \text{ V} \sim V_{CC}$	BE BELL INDERS	SHIE VIQU	2	μΑ
Operating Power Supply Current	Icc	$\overline{\text{CS}} = V_{IL}$, Output Open	Y 10	40	80	mA
	IsB	$\overline{\text{CS}} - V_{IH}$	201000	10	20	mA
Standby Power Supply Current	I_{SB1}	$\overline{CS} = V_{cc} - 0.2 V$ $V_{IN} \le 0.2 V \text{ or } \ge V_{cc} - 0.2 V$	si	lisq pal	50	μΑ
Output Low Voltage	Vol	IoL = 8 mA	-	Mili	0.4	V
Output High Voltage	Von	$I_{OH} = -4 \mathrm{mA}$	2.4		7	V

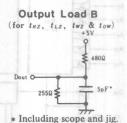
Note) Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

MAC TEST CONDITIONS

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure



* Including scope and jig.



ECAPACITANCE $(Ta=25^{\circ}\text{C}, f=1.0\text{MHz})$

Item	Symbol	typ.	max	Unit	Conditions		
Input Capacitance	Cin	3	5	pF	V _{IN} = 0 V		
Output Capacitance	Соит	5	7	pF	Vout-0V	AR MUMIXA	ABSOLUTE N

Note) This parameter is sampled and not 100% tested.

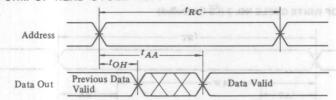
MAC CHARACTERISTICS ($Ta=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{cc}=5\text{V}\pm10\%$, unless otherwise noted.) •READ CYCLE

	Cumbal	HM616	7HLP-45	HM6167HLP-55		and the same	Notes
Item	Symbol	min	max	min	max	Unit	Notes
Read Cycle Time	tRC	45	auto mou	55	19.38 <u>0</u> 00	ns	(1)
Address Access Time	tAA	1 - ware	45		55	ns	The second
Chip Select Access Time	tACS	- 3 5	45	1000	55	ns	
Output Hold from Address Change	toH	5	70	5	enters.	ns	Yliggu?
Chip Selection to Output in Low Z	tLZ	5		5	100	ns	(2)(3)(7)
Chip Selection to Output in High Z	tHZ	0 8.0	30	0	30	ns	(2)(3)(7)
Chip Selection to Power Up Time	tPU	0	-	0	-	ns	
Chip Deselection to Power Down Time	tPD		30	-	30	ns	THE NAME OF THE OWNER,

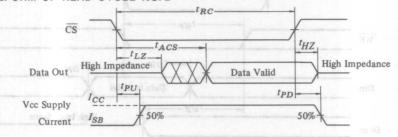
- NOTES: 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
 - 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 - 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
 - 4. WE is High for READ cycle.

 - 5. Device is continuously selected, $\overline{\text{CS}}$ = V_{IL} .
 6. Addresses valid prior to or coincident with $\overline{\text{CS}}$ transition low.
 - 7. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO. 1 4) 5)



TIMING WAVEFORM OF READ CYCLE NO. 2 4) 6)



• WRITE CYCLE

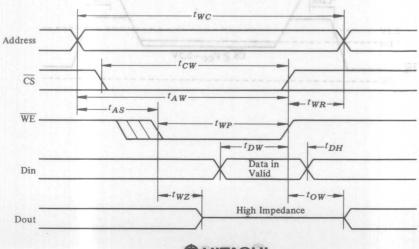
	C	HM6167	HLP-45	HM6167HLP-55		Unit	Notes
Item	Symbol	min	max	min	max	Ont	Notes
Write Cycle Time	twc	45	HMM_I JA	55	ATMBIS:	ns	(2)
Chip Selection to End of Write	tcw =	40	-	50	-	ns	
Address Valid to End of Write	tAW	40	-	50	-	ns	Jack tol Sat
Address Setup Time	tAS	0	-W ≤ 255	0	-	ns	
Write Pulse Width	tWP	25	Ly < y	35	-	ns	lata ficters
Write Recovery Time	twR	0		0	-	ns	
Data Valid to End of Write	tDW	25		25	DIVE GOLDAN	ns	DISERVINE
Data Hold Time	tDH	0		0		ns	d apprince
Write Enable to Output in High Z	twz	0	25	0	25	ns	(3) (4)
Output Active from End of Write	tow	0	-	0	-	ns	(3) (4)

NOTES: 1. If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance states.

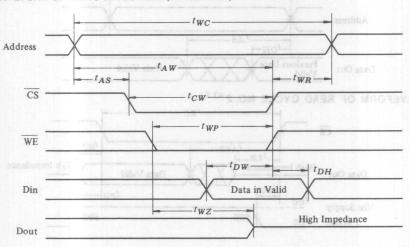
- 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.

 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
- 4. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS Controlled)



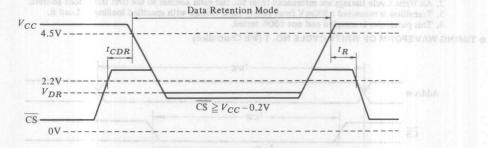
■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	TOW	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	- 02	WAR	2.0	51-1/	balk as bils	V
243	9	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{ V}$	143	_		20*	dilares S
Data Retention Current	ICCDR	$V_{i*} \ge V_{CC} - 0.2 \mathrm{V}$ or	4301		-	30**	μА
Chip Deselect to Data Retention Time	tcor	0 V ≤ V ₁ , ≤ 0.2 V	20.00.3	0	-	man i viavo	ns
Operation Recovery Time	t _R		AGI	tRC△	_		ns

△ tRC = Read Cycle Time

* Vcc-2.0V ** Vcc-3.0V

•LOW Vcc DATA RETENTION WAVEFORM



HM6264P-10, HM6264P-12, HM6264P-15

8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

Fast access Time

Low Power Standby
Low Power Operation

100ns/120ns/150ns (max.)

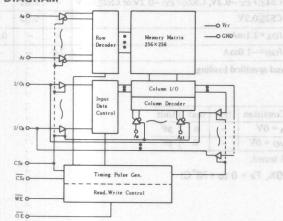
Standby: 0.1mW (typ.)
Operating: 200mW (typ.)

Single +5V Supply

- Completely Static Memory.... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

(DP-28)

BLOCK DIAGRAM

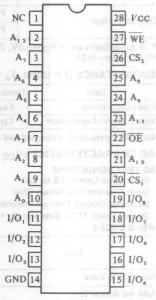


ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	VT	-0.5 ** to +7.0	V
Power Dissipation	PT	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C
Storage Temperature (Under Bias)	Toias	-10 to +85	°C

^{*} With respect to GND. ** Pul

■ PIN ARRANGEMENT



(Top View)

TRUTH TABLE

WE	CS,	CS ₂	ŌĒ	Mode	I/O Pin	V _{CC} Current	Note
X	Н	X	X	Not Selected	High Z	ISB, ISB1	
X	X	L	X	(Power Down)	High Z	ISB, ISB2	O L MOD DURAN
Н	L	Н	Н	Output Disabled	High Z	Icc, Icc1	
Н	L	Н	L	Read	Dout	Icc, Icc1	tamuo of eldenii ii.
L	L	Н	Н	Write	Din	Icc, Icc1	Write Cycle (1)
L	L	Н	L	Wille	Din	Icc, Icc1	Write Cycle (2)

^{× :} Don't care.

^{**} Pulse width 50ns: -3.0V

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
	VIH	2.2		6.0	V
Input Voltage	V_{IL}	-0.3*	_	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

				594 BE J 188	MALESCE, N	W. C. L. C.
Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	ILIIDOT	Vin=GND to VCC	aW_di	N Sta	2	μΑ
Output Leakage Current	IILO	$\overline{\text{CS1}}=V_{IH}$ or $\text{CS2}=V_{IL}$ or $\overline{\text{OE}}=V_{IH}$, $V_{I/O}=\text{GND}$ to V_{CC}		is assi i stad	2	μΑ
Operating Power Supply Current	Icc	$\overline{\text{CS1}}=V_{IL}$, $\text{CS2}=V_{IH}$, $I_{I/O}=0\text{mA}$	squink	40	80	mA
Average Operating Current	Icc1	Min. cycle, duty=100%, CS1=V _{IL} , CS2=V _{IH}	RADE N	60	110	mA
(85-30)	ISB	$\overline{\text{CS1}}=V_{IH}$ or $\text{CS2}=V_{IL}$, $I_{I/O}=0$ mA	-	1	3	mA
Standby Power Supply Current	I _{SB1**}	$\overline{\text{CS1}} \ge V_{CC} - 0.2 \text{V}$, $\text{CS2} \ge V_{CC} - 0.2 \text{V}$ or $\text{CS2} \le 0.2 \text{V}$	_[V]+	0.02	2	mA
N SPANGEMENT	ISB2**	CS2≦0.2V	-32	0.02	2	mA
0.001.001	VOL	IoL=2.1mA)-	-	0.4	V
Output Voltage	VOH	I _{OH} =-1.0mA	2.4	-	-	V

Fast access Time

* Typical limits are at Vcc=5.0V, Ta=25°C and specified loading.

** VIL min=-0.3V

CAPACITANCE $(f = 1 \text{MHz}, T_a = 25^{\circ}\text{C})$

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0V$	171	6	pF
Input/Output Capacitance	CI/O	$V_{I/O} = 0V$	1+1	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^{\circ}$ C)

• AC TEST CONDITIONS

Input Pulse Levels: 0,8 to 2.4V Input Rise and Fall Times: 10ns

Input Rise and Fall Times: Tons

Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

. READ CYCLE

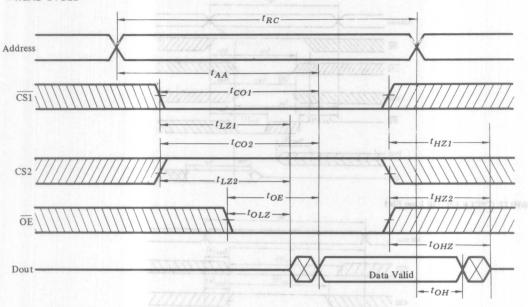
Itom	. Taki	Cumbal	HM626	4P-10	HM626	64P-12	HM62	64P-15	Crreta
Old Jan Item	.0/4	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	CIRREN	tRC	100	55 (4 =1.)	120	N 4	150	antiezedus	ns
Address Access Time		tAA	1.4	100	897	120	8 195(CU)	150	ns
Chin Selection to Output	CS1	tco1		100	E - SERVIC	120	-	150	ns
Chip Selection to Output	CS2	tCO2	-	100	-	120	-	150	ns
Output Enable to Output V	alid	toE	mil O	50	- 3	60	_L30	70	ns
Chip Selection to	CS1	tLZ1	10		10	Selected wee Dove	15	-	ns
Output in Low Z	CS2	tLZ2	10	- 1	10	ferio tua	15	it i	ns
Output Enable to Output in	Low Z	tolz	5		5	- b	0A 5	4.1	ns
Chip Deselection to	CS1	tHZ1	0	35	0	40	0	50	ns
Output in High Z	CS2	tHZ2	0	35	0	40	0	50	ns
Output Disable to Output in	High Z	toHZ	0	35	0	40	0	50	ns
Output Hold from Address Change		toH	10		10	-	15	-	ns

NOTES: $1 t_{HZ}$ and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

(I) HITACHI

2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

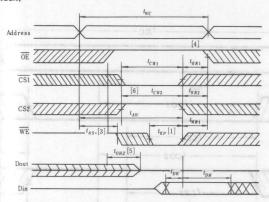


NOTE: 1) WE is high for Read Cycle

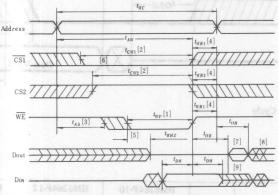
• WRITE CYCLE

*****	45.00	Country 1	HM62	64P-10	HM626	64P-12	HM62	64P-15	Unit
Item		Symbol	min	max	min	max	min	max	Unit
Write Cycle Time		twc	100	o ends at	120	ol go l og A	150	iri a ri oa	ns
Chip Selection to End of	Write	tċw	80	W One w	85	anianiwed -	100	agriorita Transasion	ns
Address Setup Time		tAS	0	Vol entos	0	d erl+ mos	0	1 31 mg1 (ns
Address Valid to End of Write		t_{AW}	80	and after or	85	our the ad	100	tizi a a 1 f	ns
Write Pulse Width		twp	60	केट दे <u>गी</u> वर्ष	70	roen <u>D</u> ro, er	90	nt at gegt (ns
Write Recovery Time	CS1, WE	t _{WR1}	5	ol gmog (5	stirW a de	10	A LEMB	ns
write Recovery Time	CS2	t _{WR2}	15	pipa <u>l</u> stat	15	saiz GV,	15	During 1	ns
Write to Output in High 2	Z	tWHZ	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	19761Z 556	50	in andra	60	low. the	ns
Data Hold from Write Time		t _{DH}	0	- 2	enbb 0 ver	ati of the	b bood on	ren a G (ns
OE to Output in High Z		toHZ	0	35	0	40	0	50	ns
Output Active from End	of Write	tow	5	-	.me/5 of	boil-43s ad	10	U UG400	ns

• WRITE CYCLE (1) (OE clock)



• WRITE CYCLE (2) (OE Low Fix)



- NOTES: 1) A write occurs during the overlap of a low CS1, a high CS2 and a low WE. A write begins at the latest transition among CS1 going low, CS2 going high and WE going low. A write ends at the earliest transition among CS1 going high, CS2 going low and WE going high. twp is measured from the beginning of write to the end of write.
 - 2) t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or CS2 going high to the end of write.
 - 3) t_{AS} is measured from the address valid to the beginning of write.
 - 4) t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high. t_{WR2} applies in case a write ends at CS2 going low.
 - 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 - 6) If CS1 goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.
 - 7) Dout is in the same phase of written data of this cycle.
 - 8) Dout is the read data of the new address.
 - 9) If CS1 is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

HM6264LP-10, HM6264LP-12 HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

Fast access Time

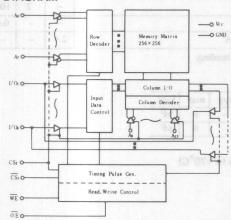
100ns/120ns/150ns (max.)

Low Power Standby
 Low Power Operation

Standby: 0.01mW (typ.)
Operating: 200mW (typ.)

- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

BLOCK DIAGRAM



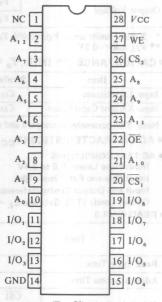
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Terminal Voltage *	VT	-0.5 ** to +7.0		
Power Dissipation	PT	1.0	W	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tstg	-55 to +125	°C	
Storage Temperature (Under Bias)	Toias	-10 to +85	°C	

^{*} With respect to GND, ** Pulse width 50ns: -3.0V

■ PIN ARRANGEMENT

(DP-28)



(Top View)

TRUTH TABLE

WE	CS ₁	CS ₂	ŌĒ	Mode	I/O Pin	V _{CC} Current	Note
X	Н	X	X	Not Selected (Power Down)	High Z	ISB, ISB1	Company of the Eastern T.
X'	X	L	X		High Z	ISB, ISB2	
Н	L	Н	Н	Output Disabled	High Z	Icc, Icc1	Output transle to Carput
H	L	OH	LO	Read	Dout	Icc, Icc1	Cris Leaderson to
L	L	Н	Н	Write	Din	Icc, Icc1	Write Cycle (1)
L	L	Н	L		Din	Icc, Icc1	Write Cycle (2)

^{× :} Don't care.

■ RECOMMENDED DC OPERATING CONDITIONS $(T_a = 0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	min	typ	max	Unit
Cumulu Walters	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Innut Valtage	VIH	2.2	_	6.0	V
Input Voltage	V_{IL}	-0.3*	-	0.8	V

^{*} Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^{\circ}$ C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	Vin=GND to VCC	_V	dus.	2	μA
Output Leakage Current	ILO	$\overline{\text{CS1}}=V_{IH}$ or $\overline{\text{CS2}}=V_{IL}$ or $\overline{\text{OE}}=V_{IH}$, $V_{I/O}=\text{GND}$ to V_{CC}	być t	ALTERNATION OF THE	2	μА
Operating Power Supply Current	Icc	$\overline{\text{CS1}}=V_{IL}$, CS2= V_{IH} , $I_{I/O}=0$ mA	300	40	80	mA
Average Operating Current	Icc1	Min. cycle, duty=100%, $\overline{\text{CS1}}=V_{IL}$, $\text{CS2}=V_{IH}$	15 × C	60	110	mA
	ISB	$\overline{\text{CS1}}=V_{IH}$ or $\text{CS2}=V_{IL}$, $I_{I/O}=0$ mA	iv endi	1 1 1	3	mA
Standby Power Supply Current	ISB1**	$\overline{\text{CS1}} \ge V_{CC} - 0.2 \text{V}$, $\text{CS2} \ge V_{CC} - 0.2 \text{V}$ or $\text{CS2} \le 0.2 \text{V}$	-	2	100	μА
THE MEDIAL OF A	ISB2**	CS2≦0.2V	-	2	100	μΑ
O-1	VOL	IOL=2.1mA	2	-	0.4	V
Output Voltage	VOH	IOH=-1.0mA	2.4	-	_	V

^{*} Typical limits are at V_{CC} =5.0V, T_a =25°C and specified loading. ** V_{IL} min=-0.3V

■ CAPACITANCE (f = 1 MHz, $T_a = 25^{\circ}\text{C}$)

A Z Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0V$	1-7	6	pF
Input/Output Capacitance	CI/O	$V_{I/O} = 0V$	-	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V\pm10\%$, $T_a = 0$ to +70°C)

• AC TEST CONDITIONS

Input Pulse Levels: 0,8 to 2,4V Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

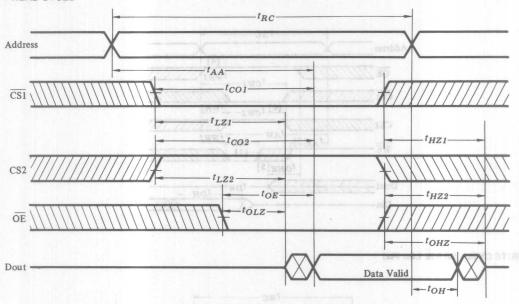
• READ CYCLE

	1381									
ON FILE Item		Symbol	HM626	54LP-10	HM626	54LP-12	HM626	4LP-15	Ilmit	
,OVI [1] Item		Syllibor	min	max	min	max	min	max	Unit	
Read Cycle Time	01	tRC	100	07 F ot 0	120	7	150	(groutnis)	ns	
Address Access Time	- GND	tAA		100	3	120	-	150	ns	
Chin Calantina to Outside	CS1	tco1		100	06	120	(Under a	150	ns	
Chip Selection to Output	CS2	tCO2	-	100	5+ Bush	120	Awa C	150	ns	
Output Enable to Output V	toE	-	50	_	60	10014	70	ns		
Chip Selection to	CS1	tLZ1	tLZ1 10 -		10	stro M_	15	0	ns	
Output in Low Z	CS2	tLZ2	10		10	bs/pelss gwod rea	15	- A	ns	
Output Enable to Output in	Low Z	tolz	5		5	risal Tare	5	-	ns	
Chip Deselection to	CS1	tHZ1	0	35	0	40	0 Re	50	ns	
Output in High Z CS2		tHZ2	0	35	0	40	0	50	ns	
Output Disable to Output in High Z		toHZ	0	35	0	40	0	50	ns	
Output Hold from Address Change		toH	10	_	10	-	15	- 11	ns	

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

² At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE



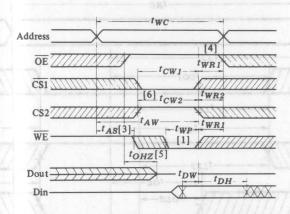
NOTE: 1) WE is high for Read Cycle

• WRITE CYCLE

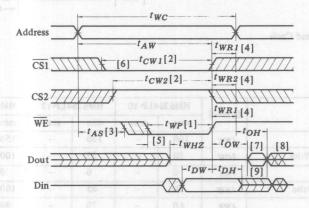
	2-11-5-5-4	0.1.	HM626	4LP-10	HM626	54LP-12	HM62	64LP-15	Unit
Item		Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	97 (17)	twc	100	1 -	120	-	150	- 1	ns
Chip Selection to End of	Write	tcw	80	70 - 17	85	Dont TT	100	_	ns
Address Setup Time	[6]	tAS	0	-	0	-	0	-	ns
Address Valid to End of	tAW	80	-	85	Din_	100	-	ns	
Write Pulse Width	tWP	60	-	70	-	90	_	ns	
W.:. D	CS1, WE	tWR1	5	_	5		10	- "	ns
Write Recovery Time	CS2	tWR2	15	-	15	-	15	-	ns
Write to Output in High 2	2	tWHZ	0	35	0	40	0	50	ns
Data to Write Time Overl	ap	tDW	40	de L b ua s	50	el a n og 9	60	els unlog	ns
Data Hold from Write Time		tDH	0	W. Ons W	0	14601, 1581 heaternion	0	Stio tes	ns
OE to Output in High Z	toHZ	0	35	0	40	0	50	ns	
Output Active from End	tow	5	med adt of	5	No out out	10	000 300	ns	

b) During the reciod, I/O pins are in the output state, therefore the input

WRITE CYCLE (1) (OE clock)



. WRITE CYCLE (2) (OE Low Fix)



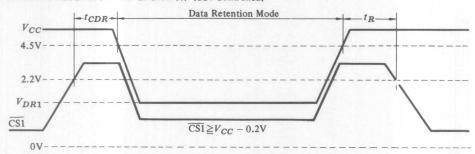
- NOTES: 1) A write occurs during the overlap of a low $\overline{\text{CS1}}$, a high CS2 and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS1}}$ going low, CS2 going high and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CS1}}$ going high, CS2 going low and $\overline{\text{WE}}$ going high. f_{WP} is measured from the beginning of write to the end of write.
 - 2) t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or CS2 going high to the end of write.
 - 3) t_{AS} is measured from the address valid to the beginning of write.
 - 4) t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at CS1 or WE going high. t_{WR2} applies in case a write ends at CS2 going low.
 - 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 - 6) If CS1 goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.
 - 7) Dout is in the same phase of written data of this cycle.
 - 8) Dout is the read data of the new address.
 - 9) If CS1 is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

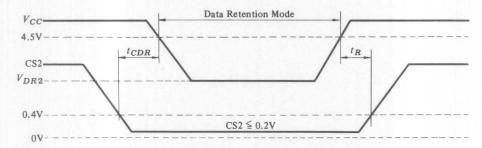
Item	Symbol	Test Condition	min	typ	max	Unit
V for Data Batantian	V_{DR1}	$\overline{\text{CS1}} \ge V_{CC} - 0.2\text{V}, \text{CS2} \ge V_{CC} - 0.2\text{V} \text{ or CS2} \le 0.2\text{V}$	2.0	-	-	V
V _{CC} for Data Retention	V_{DR2}	CS2 ≤ 0.2V	2.0	-	-	V
Data Retention Current	I _{CCDR1}	$V_{CC} = 3.0V, \overline{\text{CS1}} \ge V_{CC} - 0.2V,$ $\text{CS2} \ge V_{CC} - 0.2V \text{ or CS2} \le 0.2V$	-	1	50*	μА
Data Retention Carrent	I _{CCDR2}	$V_{CC} = 3.0 \text{V}, \text{CS2} \le 0.2 \text{V}$	-	1	50*	μA
Chip Deselect to Data Retention Time	tCDR	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R		tRC**	-	-	ns

^{*} $V_{IL} \min = -0.3 \text{V}$

• LOW Vcc DATA RETENTION WAVEFORM (1) (CS1 Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: CS_2 controls Address buffer, \overline{WE} buffer, \overline{CS}_1 buffer and \overline{Din} buffer. If CS_2 controls data retention mode, \overline{Vin} level (Address, \overline{WE} , \overline{CS}_1 , I/O) can be in the high impedance state. If \overline{CS}_1 controls data retention mode, CS_2 must be $CS_2 \ge Vcc - 0.2V$ or $CS_2 \le 0.2V$. The other inputs level (address, \overline{WE} , I/O) can be in the high impedance state.

^{**} t_{RC} = Read Cycle Time

B LOW MY DATA RETENTION CHARACTERISTICS (T. = 0 to +70 °C)

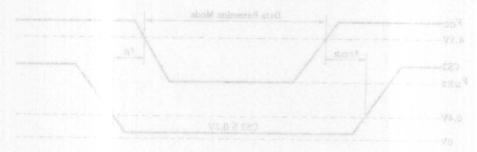
	XROL				
A			C82 ≤ 0.2V		
			$V_{CC} = 3.0V_{c} \text{ CSS} \ge V_{CC} - 0.2V_{c}$ $CSS \ge V_{CC} - 9.2V_{CC} \text{ CSS} \le 0.2V_{c}$		
Aq.					Data Recention Current
			See Resention Waveform	reak	
				R I	

^{/£.0 -} e nigr selv

E LOW VOE DATA RETENTION WAVEFORM OF 1031 Controlled)



bellowing SED (S) MROTEVAW MUSTVETER ATACLAY WOUld



VOTE: CS, concots address buffer, WE buffer, CS, buffer and Die buffer. CS, convolt data retention mode, Vin level (Address, WE, CS, 1/O) can be in the high impedance state, if CS, controls data retention mode, CS must be CS, 2 Nov-0.3 vot CS, 503. The other impure level (address WE, CS, 2 Nov-0.3 votation impure level (address WE).

away Dead Cycle Time

HMATIGA-1. HMATIGA-2, HMATIGAP-1. HMATIGAP-2, HMATIGAP-1. HMATIGAP-2, HMATIGAP-3. HMATIGAF-4.

16334-word X a bit Dynamic Random Access Memory The HMM716A is a 16,384 word by 1 bit MOS random access memory circuit haricased with HITACHI's double poly Michanist silicon gets process for high performance and high functional density. The HMM716A uses a single transistor dynamic storage cell density. The HMM716A uses a single transistor dynamic storage cell dissipation. Multiplexed address inputs permit the HMM716A to be packaged in a standard address inputs permit the HMM716A to be size provides high a standard for DIP on 0.3 inch centers. This package will be automated testing and insertion equipment. The HMM716A visit designed to facilitate upgrading of the 16-pin 4K RAM. However, appropriate for 16-K RAM's, This new generation of memory pin oducts (16-K RAM's) requires a slightly modified output stage to him with 16-K acceptated by the Column Address Storobe with remain valid from the access that from the Column Address Storobe until CE goes into prechage.

HMC A-E, HMAZIGA-E
HMC A-E, HMAZIGA-E
(DC 344)
HMAZIGAP-E
HMAZIGAP-E
HMAZIGAP-E
HMAZIGAP-E
HMAZIGAP-E

AOS DYNAMIC RAM

e all write operation are handled in the saily write mode, men data in can be concacted directly to data-out on a printed directly

2. Data Outsur Control.

Date will remain valid at the output during a read cycle from TCELOV until CE returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods or Chip Selection

Both CE and/or RE can be decoded for ahip selection.

theritall .

Refinabiling can be accomplished every 2 ms by either of the two ollowing mathods.

- (1) normal need or write cycles on 128 addresses, AD to AB.
 - (2) P i pally cycles on 128 addresses, AO to AB

A write cycle will re-train stoned data on all bits of the selected row.

RE only refreshes results in a substantial reduction in operation nower.

S Page Made Operation

The HM4716A is designed for page mode operation.



New	

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4

16384-word × 1-bit Dynamic Random Access Memory The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe (CE). Data out of the HM4716A will remain valid from the access time from the Column Address Strobe until CE goes into precharge logic 1). However, in early write cycles (W active low before CE goes low), the data output will remain in the high impedance (opencircuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

1. Common I/O Operation

If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.

2. Data Output Control

Data will remain valid at the output during a read cycle from TCELQV until $\overline{\text{CE}}$ returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods of Chip Selection

Both CE and/or RE can be decoded for chip selection.

4. Refresh

Refreshing can be accomplished every 2 ms by either of the two following methods:

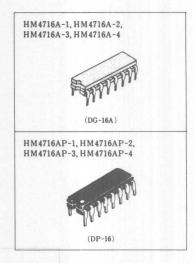
- (1) normal read or write cycles on 128 addresses, A0 to A6.
- (2) RE only cycles on 128 addresses, A0 to A6.

A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

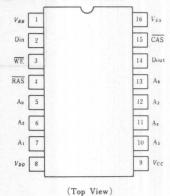
RE only refreshes results in a substantial reduction in operating power.

5. Page Mode Operation

The HM4716A is designed for page mode operation.



PIN ARRANGEMENT



Old	New	Definitions
A0-A6	A0-A6	Address Inputs
CAS	CE	Column Address Strobe
DIN	D	Data In
Dout	Q	Data Out
RAS	RE	Row Address Strobe
WRITE	W	Read/Write Input
V_{BB}	VBB	Power (-5V)
Vcc	V.C.C	Power (+5V)
V_{DD}	VDD	Power (+12V)
Vss	VSS	Ground

FEATURES

	All In	puts	Including	Clocks	TTL	Compatible
--	--------	------	-----------	--------	-----	------------

- Input Latches for Address and Data in
- Three-State TTL Compatible Output
- Common I/O Capability
- Only 128 Refresh Cycles Required Every 2ms
- Standard Power Supplies +12V, +5V, -5V (All with 10% tolelance)

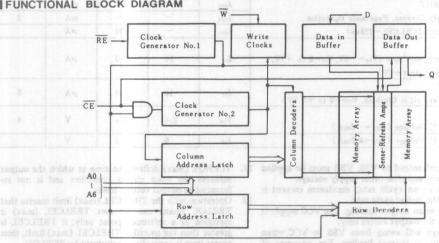
Maximum Access Time

HM4716A-1											120ns
HM4716A-2											150ns
HM4716A-3											200ns
HM47164-4											

Read or Write Cycle Time

HM4716A-1														320ns
HM4716A-2														320ns
HM4716A-3										į				375ns
HM471644					3		000	10	73			٥		410ns

FUNCTIONAL BLOCK DIAGRAM



BABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to VBB	0.5V to +20V
Voltage on VDD, VCC Supplies Relative to VSS	0.5V to +15V
Voltage on Q Pin Relative to VSS	· · -0.5V to +10V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Ambient)*	
Short-Circuit Output Current	
Power Dissipation	· · 1W
and the state of t	

■ RECOMMENDED DC OPERATING CONDITIONS (TA'= 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes					
	VDD	10.8	12.0	13.2	V	BitA					
Supply Voltage	VCC	4.5	5.0	5.5	V	101					
	VSS	0	0	0	V	1					
	VBB	-4.5	-5.0	-5.5	V						
Input High (logic 1) Voltage RE, CE, W	VIHC	2.7		6.5	V	1					
Input High (logic 1) Voltage All inputs except RE, CE, W	VIH	2.4	-	6.5	V	1					
Input Low (logic 0) Voltage all inputs	VIL	-1.0	-	0.8	V	1					

reference level for meneral

DC ELECTRICAL CHARACTERISTICS

 $(T_a=0 \text{ to } +70^{\circ}\text{C}, V_{DD}=12\text{V}\pm10\%, V_{CC}=5\text{V}\pm10\%, V_{BB}=-5\text{V}\pm10\%, V_{SS}=0\text{V})$

Parameter Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT	I_{DD1}	TuqtoO	35	m A	2
Average Power Supply Operating Current	Iccı	-	V S ilico	mA I	omm3) e
(RE, CE Cycling; TRELREL=375ns)	I_{BB1}	latited Eve	300	μΑ	1 (12) e
STANDBY CURRENT SMIT BOYO STIW TO DESPRIS	IDD2	-, V8+, V	1.500	m A	sbnar2 e
Power Supply Standby Current	Iccz	-10	10	PA TO	5
$(\overline{RE} = \overline{CE} = V_{IHC})$	I_{BB2}	-	100	μA	
REFRESH CURRENT	I_{DD3}	-	27	m A	2
Average Power Supply Current, Refresh Mode	Iccs	-10	10	μA	5
$(\overline{RE} \text{ Cycling}, \overline{CE} = V_{IHC}; \text{ TRELREL} = 375 \text{ ns})$	I_{BB3}	-	300	μA	2
PAGE MODE CURRENT	I_{DD4}	MARIO	27	mA MC	PEUNCTE
Average Power Supply Current, Page-mode Operation	Icc 4	-	-	m A	3
$(\overline{RE} = V_{IL}, \overline{CE} \text{ Cycling}; \text{ TCELCEL} = 225 \text{ns})$	I_{BB4}	-	300	μA	
INPUT LEAKAGE	IT	Loll solution	5 - 3)		
Input Leakage Current, any Input $(V_{BB} = -5V, V_{IN} = 0 \text{ to } +7V,$	IIL	-10	10	μA	
all other pins not under test = OV)					
OUTPUT LEAKAGE	,	-10	10		5
Output Leakage Current (Q is Disabled, Vour=0 to +5.5V)	IOL	-10	10	μA	3
OUTPUT LEVELS	Von	2.4	Vcc	v	4
Output High (Logic 1) Voltage (Iour=-5mA)	V OH	2.4	VCC	4	7
Output Low (Logic 0) Voltage (Iour=4.2mA)	Vol	0	0.4	V	

NOTES

- before and removed after other supply voltage.
- 2. Current depend on cycle rate: maximum current is measured at the fastest cycle rate.
- ICC depends upon output loading. The VCC supply is connected to the output buffer only.
- Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be 13. reduced to VSS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.
- 5. ICC2, ICC3 and IOL consists of leakage current only.
- 6. AC measurements assume TT = 5ns.
- 7. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VILS.
- 8. Assumes that TRELCEL = TRELCEL (max.) If TRELCEL is greater than the maximum recommended value shown in this table, TRELQV exceeds the value
- 9. Assumes that TRELCEL = TRELCEL (max).
- Measured with a load circuit equivalent to 2TTL loads 16. $\overline{CE} = VIHC$ to disable Q. and 100pF (in case of HM4716A-2:1 TTL and 50pF). And VSS + 0.8V, VSS + 2.0V are the reference level for measuring timing of Q.

- 1. All voltages referenced to VSS, VBB must be applied 11. TCEHQZ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - Operation with the TRELCEL (max) limit insures that TRELQC (max) can be met TRELCEL (max) is specified as a reference point only; if TRELCEL is greater than the specified TRELCEL (max) limit, then access time is controlled exclusively by TCELQV.
 - These parameters are reference to CE leading edge in early write cycles and to W leading edge in delayed write or read-modify-write cycles.
 - 14. TWLCEL, TCELWL and TRELWL are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if TWLCEL = TWLCEL (min), the cycle is an early write and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if TCELWL = TCELWL (min) and TRELWL will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
 - Capacitance measured with Boonton Meter or effective capacitance measuring methods.)

*READ CYCLE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, V_{DD}=12\text{V}\pm10\%, V_{CC}=5\text{V}\pm10\%, V_{SS}=0\text{V}, V_{BB}=-5\text{V}\pm10\%)$

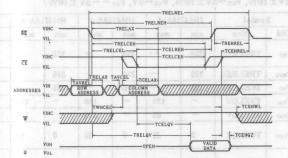
Parameter		Symbol		16A-1	27377	716A-2		716A-3		716A-4	Unit	Notes
	Old	New	min	max.	min	max	min	max	min	max		
Random Read or Write Cycle Time	t _{RC}	TRELREL	320	14120T-1	320	IRT	375	Б.	410	-	ns	
Read-Write Cycle Time	trwc	TRELREL	320	_	320	100387	375	_	515	_	ns	8
Page Mode Cycle Time	t PC	TCELCEL	160	73/24	170		225	238339001	275	_	ns	
Access Time From RE	trac	TRELQV	-	120	1-	150	-	200	-	250	ns	8, 10
Access Time From CE	tcac	TCELQV		80	-	100	700-	135	-	165	ns	9, 10
Output Buffer Turn-off Delay	toff	TCEHQZ	0	35	0	50	0	60	0	70	ns	11
Transition Time (Rise and Fall)	t _T	TT	3	35	3	35	3	50	3	50	ns	7
RE Precharge Time	trp	TREHREL	100	-	100	_	120	W Y	150	LIDYS	ns	W.
RE Pulse Width	tras	TRELREH	120	10000	150	10000	200	10000	250	10000	ns	
RE Hold Time	trsh	TCELREH	80	- 101 - 131,32 -1 -	100		135	y -	165	-	ns	
CE Pulse Width	tcas	TCELCEH	80	10000	100	10000	135	10000	165	10000	ns	
CE Hold Time	tcsH	TRELCEH	120		150	-	200	-	250	-	ns	
RE to CE Delay Time	trcd	TRELCEL	15	40	25	50	30	65	40	85	ns	12
CE to RE Precharge Time	tcrp	TCEHREL	0	1-10	-20	A PROFESSION	-20	-	-20	-	ns	
Row Address Set-up Time	tasa	TAVREL	0	7770V=2	0	W 701	0	2020 1	0	-	ns	
Row Address Hold Time	, trah	TRELAX	15	-	20	-	25	-	35	-	ns	
Column Address Set-up Time	tasc	TAVCEL	-5	100	-5		-5	_	-5	_	ns	
Column Address Hold Time	tCAH	TCELAX	40	N	45	277777	55	- 20	75	-	ns	
Column Address Hold Time Reference to RE	t _{AR}	TRELAX	80	1- Xn.13-17 I	95	Vor	120	-	160	-	ns	
Read Command Set-up Time	trcs	TWHCEL	0	1	0		0	-	0	-	ns	
Read Command Hold Time	trch	TCEHWL	0		20	_	20	V =	20	-	ns	
Write Command Hold Time	twcн	TCELWH	40	-	45	_	55	-	75	_	ns	
Write Command Hold Time Reference RE	twcr	TRELWH	80	-	95	१३ जा	120	насы	C160	STIN	ns	3A o
Write Command Pulse Width	twp	TWLWH	40	GT	45	-	55	-	75	_	ns	
Write Command to RE	trwL	TWLREH	50	1	60	-	80	21	100	_	ns	
Write Command to CE Lead Time	tcwl	TWLCEH	50		60	1891 JAJ91	80	15	100	-	ns	
Data-in Set-up Time	tos	TDVCEL	0	() () () () ()	0	W	0	ema	0	-	ns	13
Data-in Hold Time	toH	TCELDX	40	10-10	45	- 1950WF	55	-	75	-	ns	13
Data-in Hold Time Referenced RE	tohr	TRELDX	80	-	95		120	Y E	160	_	ns	
CE Precharge Time (for Page-mode Cycle Only)	tcp	TCEHCEL	60	=3 <u>40</u> -	60	-	80	(V <u>0</u>	100	-	ns	
Refresh Period	tref	TRVRV	es Period	2	an an	2	MITTER.	2	-	2	ms	
W Command Set-up Time	twcs	TWLCEL	0	-	-20	-	-20	-	-20	-	ns	14
CE to RE Delay	tcwp	TCELWL	60	_	70	-	95	wern sure	125	2 7 55 34	ns	14
RE to W Delay	trwp	TRELWL	100	_	120	-	160	-	200	-	ns	14
RE Precharge to CE Hold Time	trpc	TREHCEL	0	801 -	0	-	0	-	0	-	ns	

AC ELECTRICAL CHARACTERISTICS

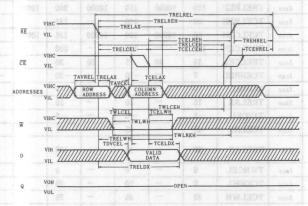
Parameter	Symbol	typ	max	Unit	Notes	
Input Capacitance (Ao-Ao, D)	Cri	3ks30T	5	pF	15	
Input Capacitance RE, CE, W	C12	- 100	10	pF	15	
Output Capacitance (Q)	Ca		7 HGV	pF	15, 16	

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4 HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4

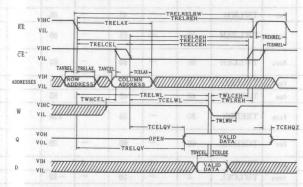
FLECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPE 2MR079WITH



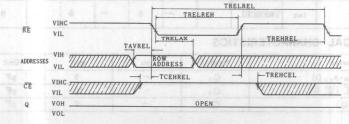
• WRITE CYCLE (EARLY WRITE)



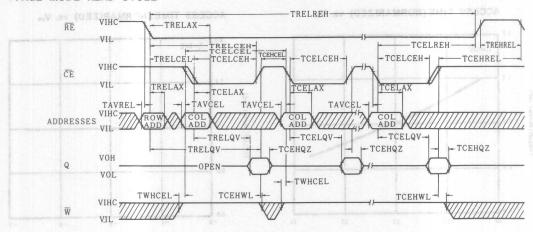
● READ-WRITE/READ-MODIFY-WRITE CYCLE



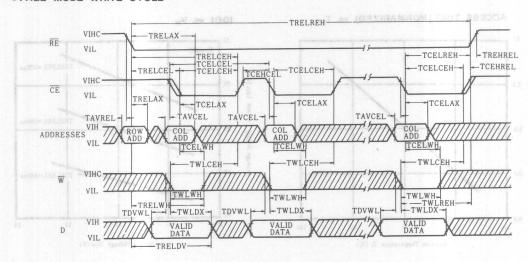
• "RE ONLY" REFRESH CYCLE



● PAGE MODE READ CYCLE

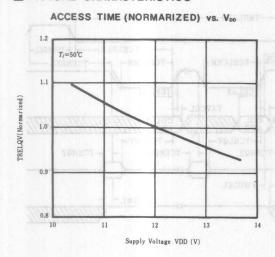


• PAGE MODE WRITE CYCLE



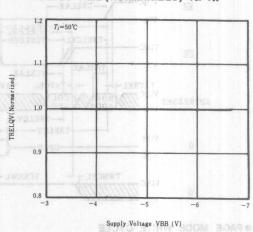


TYPICAL CHARACTERISTICS

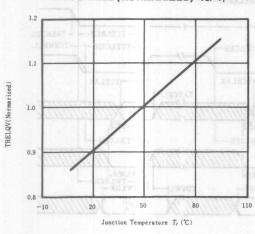


ACCESS TIME (NORMARIZED) vs. Vas

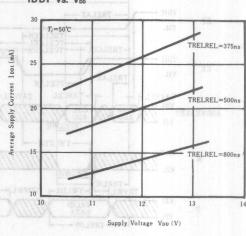
PPAGE MODE PEAD CYCLE



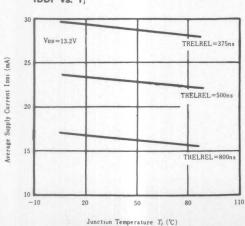
ACCESS TIME (NORMARIZED) vs. Ti



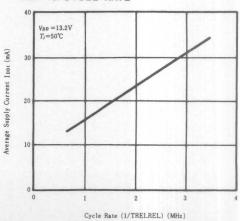
IDDI vs. VDD

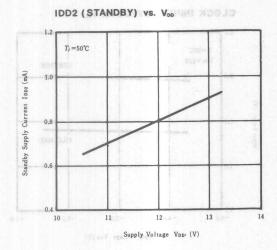


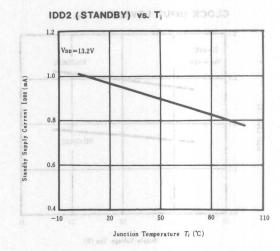
IDDI vs. Ti

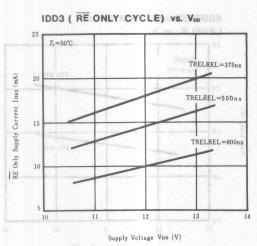


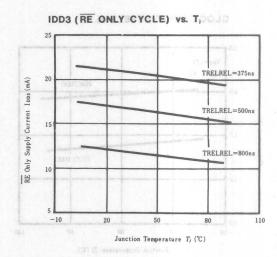
IDDI vs. CYCLE RATE

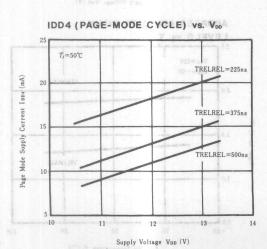


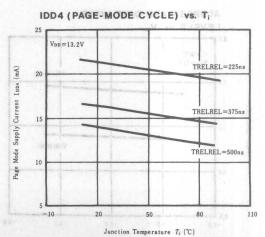




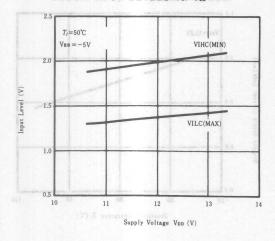




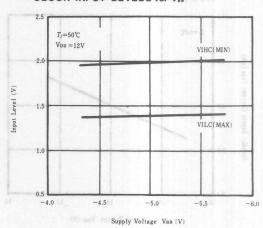




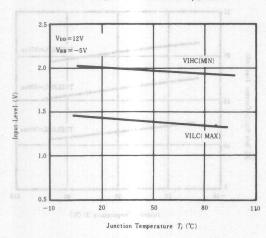
CLOCK INPUT LEVELS vs. VDD



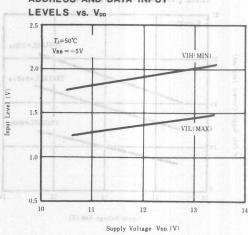
CLOCK INPUT LEVELS vs. V,



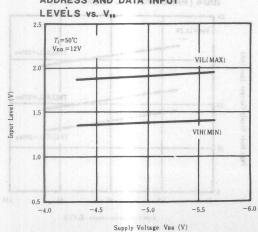
CLOCK INPUT LEVELS vs. T



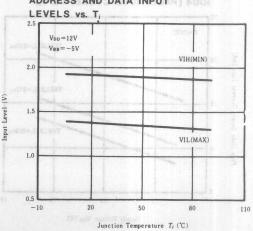
ADDRESS AND DATA INPUT



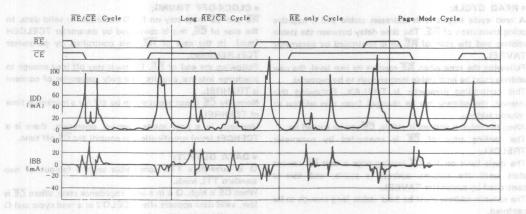
ADDRESS AND DATA INPUT



ADDRESS AND DATA INPUT



CURRENT WAVEFORMS



NOTE: VDD = 13.2V, VBB = -4.5V, $Ta = 25^{\circ}C$

- 50ns

nemary cycle at each of the 28 role addresses within each wo millipseand time is one of the country cycle in which RE remail occurs refreshes the entire interest occurs of the entire interest occurs.

The pally refresh results in a control reduction in operating owner.

The respection in power is separal in the IDDR assertion.

BOOM SOME

operations at muripie coi.

address with locenesed apexi.

This is done by probling to use address into the chip and materialing RE as a logic.

Throughout all successive CE memory cycles in which the use address is lateled. As the

eliminated, accuss ead cycle may can be decreased and the operating power to reduc. These are reflected in the TCELQV, TCELQV, TCELQV, TCELQV.

RELICEL level is not an operating limit of the HMA718A nearly fits appendication is listed on the data shears, if CE ecomes on later than TRELICEL (mark), the access time out RE will be intraced by the time which TRELICEL access TRELICEL access TRELICEL access the time when CE resolves its low level, the otherway the time when CE resolves its low level, the

era-out plus remains a a high impodernal state until a valid late appears. This is empeted is TCELQV social time from IETRELQV is the time from IETRELQV is the time from IETRELQV is the time from strived as the sun of TRELQEL(max) and TCELQV. The elected context of the is held valid internally until CE alconess high, and then Q pin becomes high impedance.

- WHITE GYCLE; A write cycle is over most by beloging W low before or laring Talon.

Two different with a cles can be defined as:

"(its cycle = Write Cate on available at the beginning of
the E.S. on to that to write operation stars at the beginning, in this most, D and W signal surface are not to any
critical parts for door making cycle time.

Collowing the time when W receives its low level. W must be resident stable long crouply to be explained. This W-on pulse duration is called TN. WH.

This cycle is called an "carly write"

Tead Write cycle — This cycle excite as a read cycle, but as boon as the device residence is mat, a write cycle is initiated. We and D an delayed until sten Q. This cycle is initiated to "delayed write" cycle is "alled a "delayed write" cycle is "alled a "delayed write" cycle in the cycle of this cycle with this cycle. A "Read-modify-write" cycle is a contained to the mode D and Wheeren

APPLICATION INFORMATION

. READ CYCLE:

A read cycle begins with addresses stable and a negative going transistion of \overline{RE} . The time delay between the stable address and the start of \overline{RE} -on is controlled by parameter TAVREL.

Following the time when RE reaches its low level, the row address must be held stable long enough to be captured.

This controlling parameter is TRELAX. Following this interval, the address can be changed from row address to column address.

When the column address is stable, $\overline{\text{CE}}$ can be turned on. The leading edge of $\overline{\text{CE}}$ is controlled by parameter

The basic limit on the CE leading edge is that CE cannot start until the column address is stable, and this is controlled by parameter TAVCEL.

The column address must be held stable long enough to be captured.

The controlling parameter is TCELAX. Note that TRELCEL(max) is not an operating limit of the HM4716A though its specification is listed on the data sheets. If $\overline{\text{CE}}$ becomes on later than TRELCEL(max), the access time from $\overline{\text{RE}}$ will be increased by the time which TRELCEL exceeds TRELCEL(max).

Following the time when $\overline{\text{CE}}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is TCELQV-access time from $\overline{\text{CE}}$. The access time from $\overline{\text{RE}}$ -TRELQV is the time from $\overline{\text{RE}}$ -on to valid Q. The minimum value of TRELQV is derived as the sum of TRELCEL(max) and TCELQV. The selected output data is held valid internally until $\overline{\text{CE}}$ becomes high, and then Q pin becomes high impedance. This parameter is TECHQZ.

· WRITE CYCLE:

A write cycle is performed by bringing \overline{W} low before or during \overline{CE} -on,

Two different write cycles can be defined as;

Write cycle — Write data are available at the beginning of the $\overline{\text{CE}}$ -on so that the write operation starts at the beginning. In this mode, D and $\overline{\text{W}}$ signal times are not in any critical path for determining cycle time.

Following the time when W reaches its low level. W must be held stable long enough to be captured. This W-on pulse duration is called TWLWH.

The time required to capture write data in a latch is called TWLDX.

This cycle is called an "early write"

Read Write cycle — This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated. \overline{W} and D are delayed until after Q. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, D and \overline{W} become critical path signals for determining cycle time.

· CLOCK-OFF TIMING;

RE and CE must stay on for Q stabilized to valid data. In the case of CE, this is controlled by parameter TCELCEH (min). In the case of RE, this controlled by parameter TCELREH(min).

Following the end of \overline{RE} , \overline{CE} must stay off long enough to precharge internal circuits. The only parameter of concern is TREHREL.

Normally $\overline{\text{CE}}$ is not required to be off for a minimum time of TCEHREL.

However, in a page mode memory operation, there is a TCEHCEL(min) specification to control the $\overline{\text{CE}}$ -off time.

· DATA OUTPUT;

 $\ensuremath{\mathbf{Q}}$ is three-state TTL compatible with a fan-out of two standard TTL loads.

When \overline{CE} is high, Q is in a high impedance state. When \overline{CE} is low, valid data appears after TCELQV at a read cycle and Q is not valid at an early-write cycle.

· REFRESH;

Refresh of the HM4716A is accomplished by performing A memory cycle at each of the 128 row addresses within each two millisecond time interval.

Any cycle in which $\overline{\text{RE}}$ signal occurs refreshes the entire selected row.

RE-only refresh results in substantial reduction in operating power.

This reduction in power is reflected in the IDD3 specification.

· PAGE MODE;

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining RE at a logic low throughout all successive CE memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are reflected in the TCELQV, TCEHCEL, IDD4 specifications.

HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7

16384-word by 1-bit Dynamic Random Access Memory The HM4816A is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816A (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power.

The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816A a truly superior RAM product. Multiplexed address inputs permits the HM4816A to be packaged in standard 16-pin DIP. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

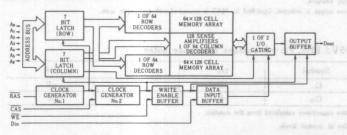
FEATURES

- Single 5V supply
 Low power standby and operation
 (Standby: 11mW max., operation: 150mW max.)
- Fast access time & cycle time

	HM4816A-3 HM4816AP-3	HM4816A-3E HM4816AP-3E		HM4816A-7 HM4816AP-7			
Maximum Access Time (ns)	100	105	A 8 120	150			
Read, Write Cycle (ns)	235	200	270	320 A ABI			
Read-Modify-Write Cycle (ns)	285	235	320	410			

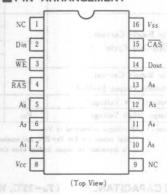
- Directly TTL compatible: All inputs & outputs
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary.
- Common I/O capability using "easy write" operation.
- Read modify write, RAS only refresh and page mode capability
- Only 128 refresh cycle required every 2ms
- Compatible with Intel 2118-3/-4/-7

■ BLOCK DIAGRAM



HM4816A-3, HM4816A-7 (DG-16B) HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7

PIN ARRANGEMENT



HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7

ABSOLUTE MAXIMUM RATINGS

Îte	m ·	Symbol	HM4816A or AP	Unit
Voltage on any pin rela	ative to GND	V_T	$-1.0 \sim +7.0$	V
Power supply voltage relative to GND		Vcc	$-0.5 \sim +7.0$	V
Short-circuit Output Current		Iout .	50	mA
Power Dissipation		P_{T}	1.0	W
Operating Temperature		Topr	0 ~ +70	°C
C. T. J.	Cerdip	T.	$-65 \sim +150$	°C
Storage Temperature Plastic		Total Tate	$-55 \sim +125$	°C

■ RECOMMENDED DC OPERATING CONDITIONS British the selection of the property o

Item specialcums som	Symbol	min	typ	max	Unit	Notes
e i soffinas va	Vcc	4.5	5.0	5.5	V	1
Supply voltage	Vss	0	0	0	V	1, 2
Input high (logic 1) voltage RAS, CAS, WE	VIHC	2.4	505 00	7.0	V	1
Input high (logic 1) voltage except RAS, CAS, WE	V_{IH}	2.4	and and A	7.0	V	1
Input low (logic 0) voltage all inputs	VIL	-2.0	-	0.8	V	1

Notes: 1. All voltage referenced to Vss.

■ DC AND OPERATING CHARACTERISTICS (1)

 $(Ta=0^{\circ}\text{C to }70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V}, \text{unless otherwise noted.})$

Parameter	Symbol	Test C	onditions	min	typ (2)	max	Unit	Notes
Input Load Current (any input)	$ I_{LI} $	$V_{IN} = V_{SS}$ to V_{CC}		97500	0.1	10	μΑ	-
Output Leakage Current for High Impedance State	$ I_{LO} $	Chip Deselected; CAS a	at V_{IH} , $V_{OUT}=0$ to 5.5V	MHT (0.1	10	μΑ	
Vcc Supply Current. Standby Icc.		CAS and RAS at VIH	HM 4816AP-3, 4, 7 HM 4816A-3, 4, 7	T	1.2	2	m A	armens h
			HM4816A, AP-3E	- +	1.2	3	m A	
N(-70)		HM4816A, AP-3 $t_{RC} = t_{I}$	CMIN	+	23	27	m A	3
V Sunda Cumant Onestina	,	HM 4816A, AP-3E t_{RC} = t_{RCMIN}			27	35	m A	3
Vcc Supply Current. Operating	I _{CC2}	HM4816A, AP-4 $t_{RC} = t_R$	CMIN	+	21	25	m A	3
		HM 4816A, AP-7 $t_{RC} = t_R$	CMIN	1111	19	23	m A	3
16 Va	758	HM4816A, AP-3 $t_{RC} = t_R$	CMIN	575	16	18	m A	3
Vcc Supply Current;		HM4816A, AP-3E tRC=t	RCMIN	-	20	25	m A	3
RAS-Only Cycle	I_{CC3}	HM4816A, AP-4 $t_{RC}^* = t_R$	CMIN	HOS BITT	14	16	m A	3
med M		HM4816A, AP-7 $t_{RC} = t_R$	CMIN	-	12	14	m A	3
Vcc Supply Current. Standby. Output Enabled	Iccs	CAS at VIL, RAS at	Vin pag bas defre	sing e	3	6	m A	3
Output Low Voltage	VOL	$I_{OL}=4.2\mathrm{mA}$	0	BY SEC YE	0.4	V	InO 8	
Output High Voltage	· V _{OH}	$I_{OH} = -5 \mathrm{mA}$	1-1	2.4	nt <u>e</u> l 21	Vcc	V	m3. 0

Notes: 1. All voltages referenced to Vss.

CAPACITANCE ($Ta=25^{\circ}\text{C}$, $V_{cc}=5\text{V}\pm10\%$, $V_{ss}=0\text{V}$, unless otherwise noted.)

Parameter	Symbol	typ	max	Unit
Address. Data In	Cri	3	5	pF
RAS, CAS, WE, Data Out	C12	4	7 TOTAL TOTAL TOTAL	pF

Notes: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

 $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.



^{2.} Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

^{2.} Typical values are for Ta=25°C and nominal supply voltages.

^{3.} Icc is dependent on output loading when the devices output is selected. Specified Icc MAX is measured with the output open.

■ AC CHARACTERISTICS (1,2,3) ($Ta=0^{\circ}$ C to 70° C, $V_{cc}=5V\pm10\%$, $V_{ss}=0V$, unless otherwise noted.)

• READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Parameter	Symbol	HM 481	16A-3 16AP-3	HM 481	6A-3E 6AP-3E	HM 48	16A-4 16AP-4	HM 48	16A-7 16AP-7	Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	min	max	Unit	DA S
Access Time From RAS	trac	100 J III 10	100	181 <u>K</u> 91	105	1 18 7 %	120	33 <u>5</u> 0	150	ns	4, 5
Access Time From CAS	10 8180 CO	bana di	55	total 1	60	ol lien	65	nodi (80	ns	4, 5, 6
LIMBO CONTRACTOR CONTRACTOR OF THE PARTY OF	t _{CAC}	FAMILIER		_	2	(.xem)	2	105025	2	ms	4, 0, 0
Time Between Refresh	tref	OWEN	2		_		-	105	5 -		CA I
RAS Precharge Time	t _{RP}	110	-	70	_	120	1	135	20.74	ns	
(non-page cycles)	tCPN	50	000 -	50	_	55		70		ns	
CAS to RAS Precharge Time	tcrp	0	Det -	0	_	0		0	51 10 8 50 1	ns	ANDER
RAS to CAS Delay Time	t _{RCD}	25	45	25	45	25	55	25	70	ns	ANT
RAS Hold Time	trsh	70	_	60	_	85	-	105	9.40	ns	AIR
CAS Hold Time	tcsH	100	21.61	105	-	120		165		ns	
Row Address Set-up Time	tasa	0	-	0	-	0	15	0	782	ns	
Row Address Hold Time	t _{RAH}	15		15		15	20-	15	- 1	ns	
Column Address Set-up Time	tasc	0	-	0	4111	0		0	_	ns	
Column Address Hold Time	tCAH	15		25	(n) -	20		20	162	ns	
Column Address Hold Time to RAS	t _{AR}	60		70	-	75	-	90	197	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	8
Output Buffer Turn Off Delay	toff	0	45	0	50	0	50	0	60	ns	
READ AND REFRESH CYC	LES			11110		A.3		2.0	You man		
Random Read Cycle Time	t _{RC}	235	-	200	40	270		320	- M-	ns	
RAS Pulse Width	tras	115	10000	105	10000	140	10000	175	10000	ns	
CAS Pulse Width	tcas	55	10000	60	10000	65	10000	95	10000	ns	
Read Command Set-up Time	tRCS	0	_	0	-	0	-	0	197	ns	
Read Command Hold Time	t _{RCH}	10		10	_	10	m2 -	10	1/2	ns	
WRITE CYCLE											
Random Write Cycle Time	t _{RC}	235	-	200	-	270	-	320	3304	ns	17111
RAS Pulse Width	tras	115	10000	105	10000	140	10000	175	10000	ns	
CAS Pulse Width	tcas	55	10000	60	10000	65	10000	95	10000	ns	
Write Command Set-up Time	twcs	0		0		0	- 11	0	157	ns	9
Write Command Hold Time	twch	25		30	1997	30	- P	45	_	ns	
Write Command Hold Time to RAS	twcn	70	-	75	70 -	85	11-1	115	-	ns	
Write Command Pulse Width	twp	25	_	30	_	30	_	50	47	ns	
Write Command to RAS Lead Time	t _{RWL}	60	_	45	1	65	-	110	_	ns	
Write Command to CAS Lead Time	*t _{CWL}	45	_	45	13/-	50	8 0	100		ns	
Data-in Set-up Time	tos	0	263 -	0	1	0	100	0		ns	
Data-in Hold Time	t _{DH}	25*		30	-	30		45		ns	
Data-in Hold Time to RAS	t _{DHR}	70		75	10.77	85	_	115	2804	ns	-
• READ-MODIFY-WRITE CYC		1 0 30		75	8	00		113	on of	113	
Read-Modify-Write Cycle Time	t _{RWC}	285	_	235	-1	320		410	-cr 969	ns	
RMW Cycle RAS Pulse Width	traw	165	10000	155	10000	190	10000	265	10000	ns	
RMW Cycle CAS Pulse Width	tcrw	105	10000	110	10000	120	10000	185	10000	ns	
RAS to WE Delay	-	100	10000		10000		10000		10000	1000	9
CAS to WE Delay	t _{RWD}	55		105		120		150		ns	
	tcwp	1 22		60		65		80	_	ns	9

3.4. VOH. M/r: and VOL. MAX are reference levels for measuring timing of Dours.
5. LOFFE is measured to LOUT < LIFE.
6. LOFFE is measured to LOUT < LIFE.
6. LOFFE is necessary to LOUT < LIFE.

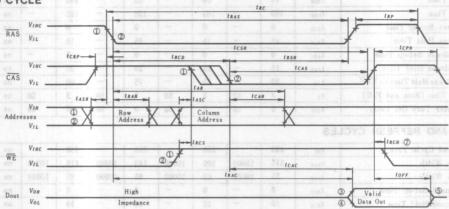
HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7 HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7

- 1. All voltages referenced to V_{SS} 2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purposes.
- 3. AC Characteristics assume t_T =5ns
- 4. Assume that $t_{RCD} \le t_{RCD}$ (max.) If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.)
- 5. Load = 2 TTL Loads and 100pF
- 6. Assumes $t_{RCD} \ge t_{RCD}$ (max.)

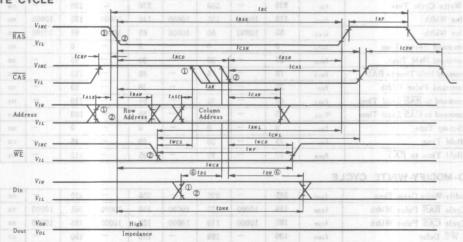
- 7. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC} . If t_{RCD} is greater than t_{RCD} (max.) access time is t_{RCD} + tCAC.
- 8. t_T is measured between V_{IH} (min.) and V_{IL} (max.)
- 9. twcs, tcwp and tRwp are specified as reference points only. If $t_{WCS} \ge t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \ge t_{CWD}$ (min.) and $t_{RWD} \ge t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address if neither of the above conditions is satisfied, the condition on the data out is indeterminate.

WAVEFORMS

OREAD CYCLE



• WRITE CYCLE

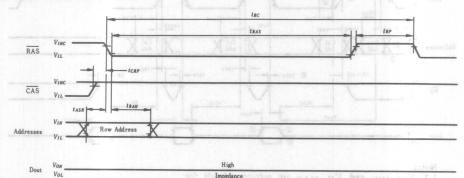


Notes:

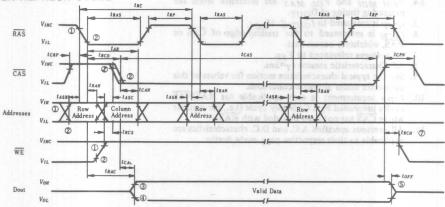
- 1.2. VIH MIN and VIL MAX are reference levels for measuring timing of input signals.
- 3.4. VOH MIN and VOL MAX are reference levels for measuring timing of DOUT.
- 5. t_{OFF} is measured to $I_{OUT} < |I_{LO}|$.
- 6. t_{DS} and t_{DH} are referenced to \overline{CAS} or \overline{WE} , whichever occurs last.
- t_{RCH} is referenced to the trailing edge of $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$, whichever occurs first.
- 8. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a \overline{CAS} -only cycle (i.e., for system where CAS has not been decoded with RAS).

• READ-MODIFY-WRITE CYCLE trrw trp 2 RAS VIL terp VIH CAS VIL tcwL Addresses 0 WE 0 6 tos-Din LOFF 3 (5) Valid Data Out

• RAS-ONLY REFRESH CYCLE



• HIDDEN REFRESH CYCLE



Notes:

- 1.2. V_{IH} M_{IN} and V_{IL} M_AX and reference levels for measuring timing of input signals.
 3.4. V_{OH} M_{IN} and V_{OL} M_AX are reference levels for measuring timing of D_{OUT}.
 5. t_{OFF} is measured to I_{OUT} ≤ |I_{LO}|
 6. t_{DS} and t_{DH} are referenced to CAS or WE, whichever occurs lest
 - occurs last.
- t_{RCH} is referenced to the trailing edge of CAS or RAS, whichever occurs first.
 t_{CRP} requirement is only applicable for RAS/CAS cycles preceded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).

DC AND AC CHARACTERISTICS, PAGE MODE (7.8.)

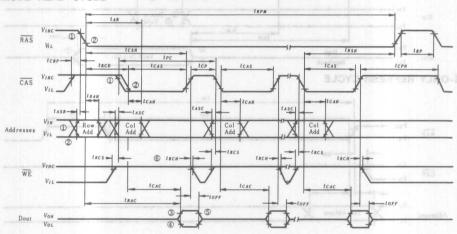
 $(Ta=0^{\circ}\text{C} \text{ to } 70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V}, \text{unless otherwise noted.})$

Parameter	Symbol	HM4816A-3 HM4816AP-3		HM 4816A - 3E HM 4816AP - 3E		HM4816A-4 HM4816AP-4		HM 4816A-7 HM 4816AP-7		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Page Mode Read or Write Cycle	t _{PC}	125	-	130	7779-70	145	1 1 -	190	213 T	ns
Page Mode Read Modify Write Cycle	t PCM	175	-	180	-	200	-	280	-	ns
CAS Precharge Time, Page Cycle	tcp	60	741	60	3000	70	popular de	85	-	ns
RAS Pulse Width, Page Mode	trpm	115	10000	105	10000	140	10000	175	10000	ns
CAS Pulse Width	tcas	55	10000	60	10000	65	10000	95	10000	ns
V _{DD} Supply Current Page Mode. Minimum t _{PC} . Minimum t _{CAS}	I_{DD4}	_	23		23	(O)	21		18	m A

WHEAD-MODIFY-WRITE CYCLE

3.4. VOH MIN and VOL MAX are ve mensyring timing of DOUT. 5. (OFF) is measured to LOUT. § (LO)

• PAGE MODE READ CYCLE

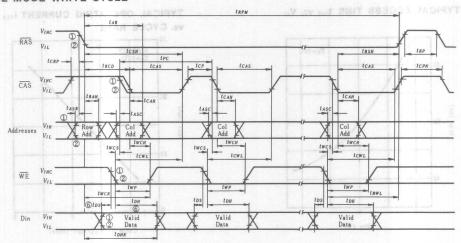


Notes:

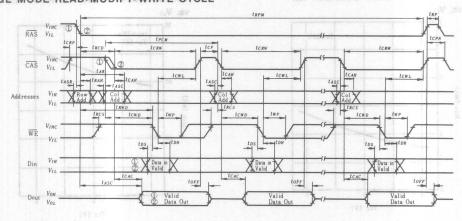
- 1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
- 3.4. V_{OH} MIN and V_{OL} MAX are reference levels for measuring timing of D_{OUT}.
 5. t_{OFF} is measured to I_{OUT} ≤ |I_{LO}|.
 6. t_{RCH} is referenced to the trailing edge of CAS or RAS, whichever occurs first.
- 7. All voltages referenced to V_{SS} . 8. AC Characteristic assume t_T =5ns.
- 9. See the typical characteristics section for values of this parameter under alternate conditions.
- t_{CRP} requirement is only applicable for RAS/CAS cycles preceded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).
- 11. All previous specified A.C. and D.C. characteristics are applicable to their respective page mode device.

tpcyr is referenced to ILAS, whichever exem:

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



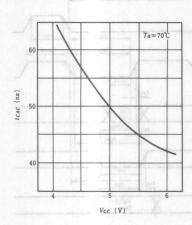
- 1.2. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals.
 - 3.4. V_{OH} MIN and V_{OL} MAX are reference levels for measuring timing of D_{OUT} .

 5. t_{OFF} is measured to $I_{OUT} \le |I_{LO}|$.

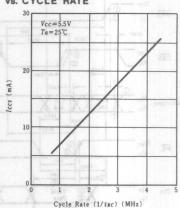
 6. t_{DS} and t_{DH} are referenced to \overline{CAS} or \overline{WE} , whichever
 - occurs last.
 - 7. t_{RCH} is referenced to the trailing edge of $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$, whichever occurs first.
 - 8. t_{CRP} requirement is only applicable for RAS/CAS, cycles preceded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).

Typical Characteristics of HM4816A

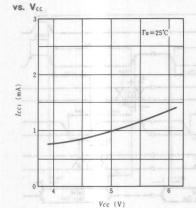
TYPICAL ACCESS TIME touc VS. Vcc



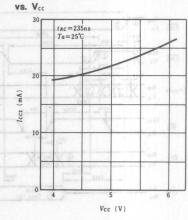
TYPICAL OPERATING CURRENT ICC2 VS. CYCLE RATE



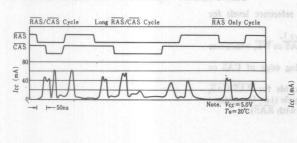
TYPICAL STANDBY CURRENT Icci



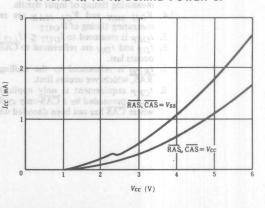
TYPICAL OPERATING CURRENT Icca



TYPICAL SUPPLY CURRENT WAVEFORMS



TYPICAL Icc vs. Vcc DURING POWER UP



HM4864-2, HM4864-3 HM4864P-2, HM4864P-3

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

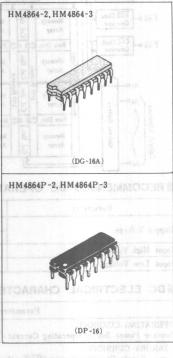
This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{\text{RAS}}$ -only refresh.

Proper control of the clock inputs (RAS, CAS, and WE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, and Page-mode capability
- 128 refresh cycle



■ PIN ARRANGEMENT

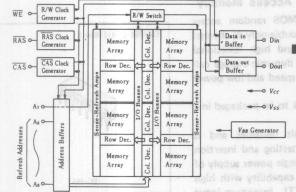


(Top View)

A 0-A 7	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
A 0 - A 6	Refresh Address Input



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative

to V_{SS}-1.0 to +7V

Operating Temperature, Ta

→ v_{ss} (Ambient) 0 to +70°C

Storage Temperature 1 no 910 mig 31 biglings

e Read-Modify-Write, RAS-only refresh, and Page-mode capability

(Ambient) -65 to +150°C (Cerdip)

-55 to +125°C (Plastic) Short-circuit Output Current . 50 mA

Power Dissipation 1 W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	Vcc	4.5	5.0	5.5	V	eneropris
	Vss	0	0	0	V	ROSNIH -
Input High Voltage	V _{IH}	2.4	arrania min	6.5	V	1,00
Input Low Voltage	VIL	-1.0		0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

Parameter AS	Symbol	u min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling; trc=min.)	Iccı	tib ovid	60	m A	2, 4
$ \begin{array}{l} {\tt STANDBY\text{-}CURRENT} \\ {\tt Power \ Supply \ Standby \ Current} \ (\overline{RAS} = V_{lib}, {\tt Dout = High \ Impedance}) \end{array} $	Iccz	-	3.5	m A	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = V _{IH} ; t _{RC} = min.)				m A	The same of the sa
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation (RAS = V _{I,I} , CAS Cycling; t _{PC} = min.)	Icca			m A	2, 4
INPUT LEAKAGE Input Leakage Current, any Input $(V_{in} = 0 \text{ to } +6.5\text{ V}, \text{ all other pins not under test} = 0\text{ V})$	I _{LI}	-10	10	μA	i edT e knisos
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, $V_{\rm exf} = 0$ to $+5.5\mathrm{V}$)	ILO	2/-10/0	10	μА	uo103 6
OUTPUT LEVELS Output High (Logic 1) Voltage (I _{vet} = -5mA) Output Low (Logic 0) Voltage (I _{out} = 4.2mA)	Von Vol	2.4	V _{cc} 0.4	v v	ary Some

NOTES

1. All voltages referenced to VSS.

2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.

I_{LO} consists of leakage current only.
 Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-A7, Din)	Cin 1		7	pF	1
Input Capacitance (RAS, CAS, WE)	Cin 2	_	10	pF	1
Output Capacitance (Dout)	Cout	-	7	pF	1, 2

1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable DOUT.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS 13, 23

 $(T_a=0 \text{ to } +70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

D	C1	HM 4864-2/P-2		HM 4864-3/P-3		Unit	Nets	
Parameter	Symbol	Symbol min max	max	min	max	Unit	Notes	
Random Read or Write Cycle Time	t _{RC}	270		335	N 773	ns		
Read-Write Cycle Time	t _{RWC}	270	-	335	-	ns		
Page Mode Cycle Time	t _{PC}	170	-	225	W SAS	ns	16/15	
Access Time from RAS	trac	-	150	-	200	ns	4,6	
Access Time from CAS	tcac	11/->	100		135	ns	5, 6	
Output Buffer Turn-off Delay	toff	0	40	0	50	ns	7	
Transition Time (Rise and Fall)	t _T	3	35	3	50	ns	3	
RAS Precharge Time	t _{RP}	100	-	120	-	ns		
RAS Pulse Width	tras	150	10000	200	10000	ns		
RAS Hold Time	t _{RSH}	100	-	135	-	ns	7,1	
CAS Pulse Width	tcas	100	-	135	-	ns	STISW	
CAS Hold Time	t_{CSH}	150	-,	200	-	ns		
RAS to CAS Delay Time	tRCD	20	50	25	65	ns	8	
CAS to RAS Precharge Time	tcrp	-20	75	-20	W	ns		
Row Address Set-up Time	task	0		0	-	ns		
Row Address Hold Time	t _{RAH}	20	-	25	283	ns		
Column Address Set-up Time	tasc	-10	estation to	-10		ns		
Column Address Hold Time	t _{CAH}	45	tessible vol	55	resist.	ns		
Column Address Hold Time referenced to RAS	t _{AR}	95	-	120		ns		
Read Command Set-up Time	t _{RCS}	0	-	0	- 62	ns		
Read Command Hold Time	t _{RCH}	0		0	38 -	ns		
Write Command Hold Time	twcH	45		55	-	ns		
Write Command Hold Time referenced to RAS	twcr	95	-	120	-	ns		
Write Command Pulse Width	twp	45		55	810	ns		
Write Command to RAS Lead Time	t _{RWL}	45	-	55	T	ns		
Write Command to CAS Lead Time	t _{CWL}	45	-	55	-	ns		
Data-in Set-up Time	tDS	0	-1	0	-	ns	9	
Data-in Hold Time	t _{DH}	45	2 3749	55	M-0/4	ns	9	
Data-in Hold Time referenced to RAS	t _{DHR}	95	-	120	-	ns		
CAS Precharge Time (for Page-mode Cycle Only)	t_{CP}	60		80	_	ns		
Refresh Period	tref	41 b	2	- N	2	ms		
Write Command Set-up Time	twcs	-20		-20	-	ns	10	
CAS to WE Delay	tcwp	60	-	80	P40 -	ns	10	
RAS to WE Delay	t _{RWD}	110	100000000000000000000000000000000000000	145		ns	10	
RAS Precharge to CAS Hold Time	l _{RPC}	0	-	0	-	ns		

NOTES

1. AC measurements assume $t_T = 5$ ns.

2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.

Assumes that $t_{RCD} \le t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.

5. Assumes that t_{RCD} ≥ t_{RCD} (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.

7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Operation with the t_{RCD} (max) limit insures that

 t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC} .

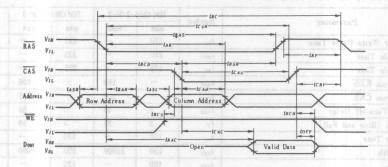
9. These parameters are reference to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed

write or read-modify-write cycles.

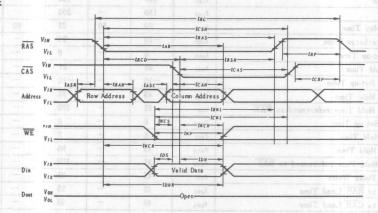
10. twcs. tcwp and trwp are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge$ trwn (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeter-

WELECTRICAL COMPACTERISTICS AND RECOMMENDED AC OPERSMONDAINT

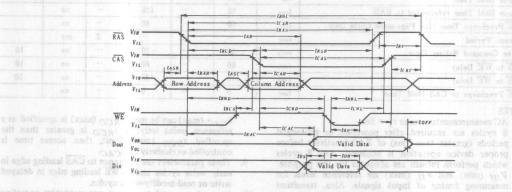
• READ CYCLE



• WRITE CYCLE



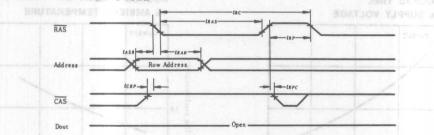
• READ-WRITE/READ-MODIFY-WRITE CYCLE



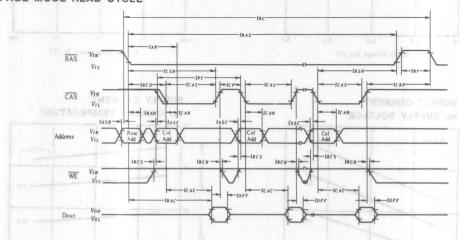
regit from the selected cell; if

MITYPICAL CHARACTERISTICS

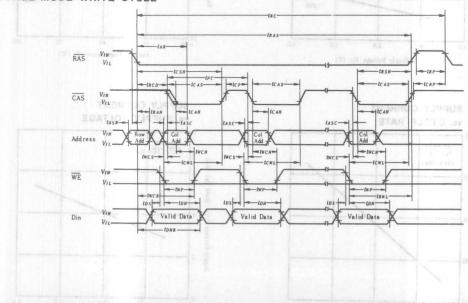
•"RAS-ONLY" REFRESH CYCLE



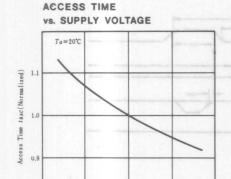
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

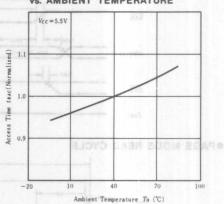


TYPICAL CHARACTERISTICS



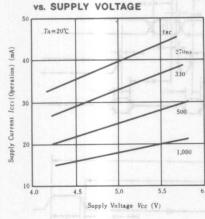
Supply Voltage Vcc (V)

ACCESS TIME TEMPERATURE

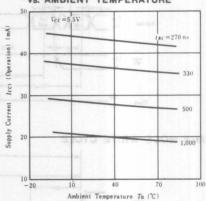


SUPPLY CURRENT

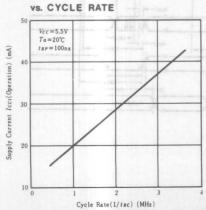
4.0



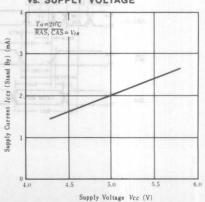
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



SUPPLY CURRENT VS. CYCLE RATE

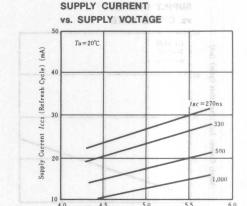


SUPPLY CURRENT vs. SUPPLY VOLTAGE

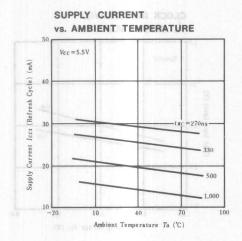


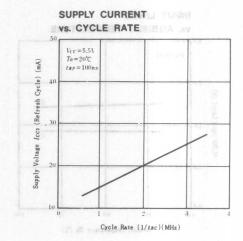
Ambient Temperature Ta (℃)

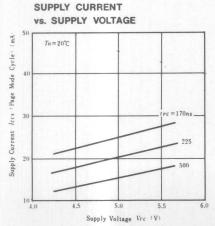
SUPPLY CURRENT

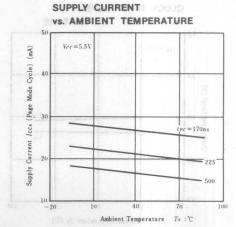


Supply Voltage Vcc (V)

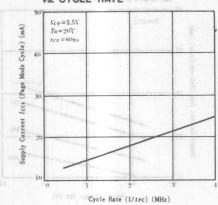




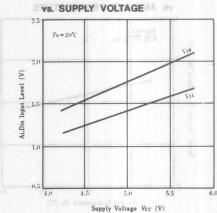




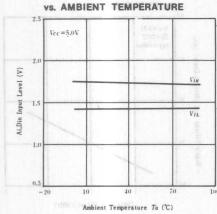
SUPPLY CURRENT VS. CYCLE RATE



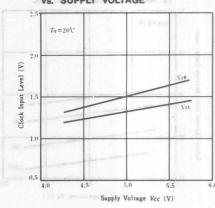
INPUT LEVEL SUO YARRING



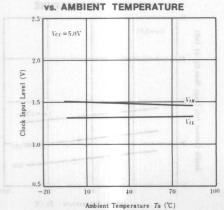
INPUT LEVEL

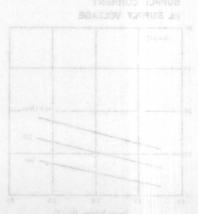


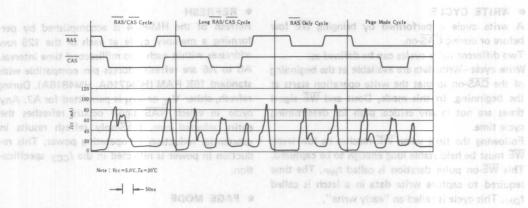
CLOCK INPUT LEVEL VS. SUPPLY VOLTAGE



CLOCK INPUT LEVEL







APPLICATION INFORMATION

POWER ON

An initial pause of 500 μ s is required after power-up and a minimum of eight (8) initialization cycle, (any combination of cycles containing a RAS clock such as RAS-only refresh) must follow an initial pause.

The V_{CC} current (I_{CC}) requirement of the HM4864 during power on is, however, dependent upon the input levels (RAS, CAS) and the rise time of V_{CC} , as shown in Fig. 1.

• READ CYCLE

to valid Dout.

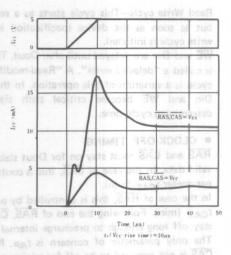
A read cycle begins with addresses stable and a negative going transition of \overline{RAS} . The time delay between the stable address and the start of \overline{RAS} -on is controlled by parameter t_{ASB} .

Following the time when \overline{RAS} reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is t_{RAH} . Following this interval, the address can be changed from row address to column address. When the column address is stable, \overline{CAS} can be turned on. The leading edge of \overline{CAS} is controlled by parameter t_{RCD} . The basic limit on the \overline{CAS} leading edge is that \overline{CAS} can not start until the column address is stable, and this is controlled by parameter t_{ASC} . The column address must be held stable long enough to be captured. The controlling parameter is t_{CAH} . Note that t_{RCD} (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If \overline{CAS} becomes on later than t_{RCD} (max), the access time from \overline{RAS} will be increased by the time which t_{RCD} exceeds t_{RCD} (max).

Following the time when \overline{CAS} reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is t_{CAC} -access time from \overline{CAS} . The access time from \overline{RAS} - t_{RAC} -is the time from \overline{RAS} -on

The minimum value of t_{RAC} is derived as the sum of t_{RCD} (max) and t_{CAC} .

The selected output data is held valid internally until $\overline{\text{CAS}}$ becomes high, and then Dout pin becomes high impedance. This parameter is t_{OFF} .



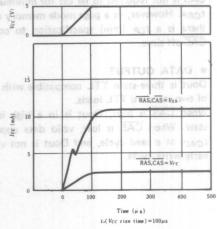


Fig.1 Icc vs. Vcc during power up.



WRITE CYCLE

A write cycle is performed by bringing WE low before or during CAS-on.

Two different write cycles can be defined as;

Write cycle—Write data are available at the beginning of the $\overline{\text{CAS}}$ -on so that the write operation starts at the beginning. In this mode, Dout and $\overline{\text{WE}}$ signal times are not in any critical path for determining cycle time.

Following the time when \overline{WE} reaches its low level, \overline{WE} must be held stable long enough to be captured. This \overline{WE} -on pulse deration is called t_{WP} . The time required to capture write data in a latch is called t_{DH} . This cycle is called an "early write".

Read Write cycle—This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

WE and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and WE become critical path signals for determining cycle time.

CLOCK-OFF TIMING

RAS and \overline{CAS} must stay on for Dout stabilized to valid data. In the case of \overline{CAS} , this is controlled by parameter t_{CAS} (min).

In the case of RAS, this is controlled by parameter t_{CAS} (min). Following the end of RAS, CAS must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP} . Normally CAS is not required to be off for minimum time of t_{CRP} . However, in a page mode memory operation, there is a t_{CP} (min) specification to control the CAS-off time.

DATA OUTPUT

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When \overline{CAS} is high, Dout is in a high impedance state. When \overline{CAS} is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid as an early-write cycle.

REFRESH

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either V_{1L} or V_{1H} is permitted for A7. Any cycle in which RAS signal occurs refreshes the entire selected row. RAS-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the *I_{CC3}* specification.

PAGE MODE

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining RAS at a logic low throughout all successive CAS memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be descreaded and the operating power is reduced. These are specifications.

The minimum value of teac is derived as the sum of teach

HM4864CC-2, HM4864CC-3

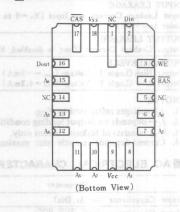
65536-word × 1-bit Dynamic Random Access Memory

FEATURES

- 18-pin Leadless Chip Carrier
- 150ns access time, 270ns cycle (HM4864CC-2)
 200ns access time, 335ns cycle (HM4864CC-3)
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low power: 330mW active, 20mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge.
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary.
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only Refresh, and Page-mode capability 128 refresh cycle

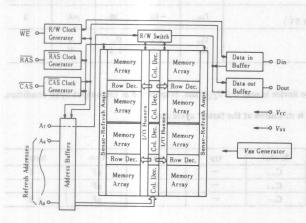


PIN ARRANGEMENT



A 0-A 7	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
A 0 - A 6	Refresh Address Input

FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative	
to V _{SS}	-1.0 to +7V
Operating Temperature, Ta	
(Ambient)	0 to +70°C
Storage Temperature	
(Ambient)	-65 to +150°C
Short-circuit Output Current .	
Power Dissipation	1 W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
	Vcc	4.5	5.0	5.5	V	1
Supply Voltage	V_{ss}	0	0	0	V	BEATURES
Input High Voltage	V _{IH}	2.4	-	6.5	s Did Vissel	18 pin Lead
Input Low Voltage	VIL	-1.0	M894CC-2)	0.8	stirV 220n	21006 21081 W

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

Parameter (MBIRI) W	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling; t RC = min.)	Iccı	WoL'sto	60	m A	2, 4
STANDBY CURRENT Power Supply Standby Current (RAS - V _{IB} , Dout - High Impedance)	Iccz	by_CAS	3.5	m A	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = V _{IH} ; t _{RC} = min.)	Iccs	et' <u>po</u> lar 1 ykno-l	45	m A	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation $\overline{(RAS} = V_{IJ}$, \overline{CAS} Cycling; $t_{PC} = \min$.)	Icc4	-	45	m A	2, 4
INPUT LEAKAGE Input Leakage Current, any Input (V., =0 to +6.5V, all other pins not under test =0V)	Iu MAR	-10	30.10	μA	DIABE
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, Vox. = 0 to +5.5V)	ILO	-10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage (I _{out} = -5mA) Output Low (Logic 0) Voltage (I _{out} = 4.2mA)	V _{OH} V _{OL}	2.4	V _{cc} 0.4	v v	L. THE
19, 58	- July 1 County		1	1000110	10

All voltages referenced to V_{SS}.
 I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.

3. I_{LO} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-Ar, Din)	Cin1	-	7	pF	1
Input Capacitance (RAS, CAS, WE)	Cin 2		10	pF	1
Output Capacitance (Dout)	Cont	- 1-1	7	pF	1, 2

WASSOLUTE MAXIMUM RATINGS

Storage Temperature

1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable D_{OUT}.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS 13, 23

 $(T_a=0 \text{ to } +70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

D	C 1 1	HM486	4CC-2	HM4864CC-3		Unit	Notes
Parameter	Symbol	min	max	min	max	Unit	Notes
Random Read or Write Cycle Time	t _{RC}	270	/	335	243	ns	
Read-Write Cycle Time	trwc	270	-	335	-	ns	
Page Mode Cycle Time	tpc	170		225	165 Pin	ns	
Access Time from RAS	trac	d to -	150		200	ns	4,6
Access Time from CAS	tcac	38-3	100	01 X	135	ns	5, 6
Output Buffer Turn-off Delay	toff	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t _T	3	35	3	50	ns	3
RAS Precharge Time	t _{RP}	100		120	- L	ns	
RAS Pulse Width	tras	150	10000	200	10000	ns	
RAS Hold Time	t _{RSH}	100	-	135	-	ns	
CAS Pulse Width	tcas	100	-	135	-	ns	BTIEW
CAS Hold Time	tcsH	150		200	-	ns	
RAS to CAS Delay Time	tRCD	20	50	25	65	ns	8
CAS to RAS Precharge Time	tcrp	-20		-20	AV TO	ns	
Row Address Set-up Time	tasa	0	- Constant	0	-	ns	
Row Address Hold Time	trah	20	+	25	F 685	ns	
Column Address Set-up Time	tasc	-10	60-9131-0e	-10	-	ns	
Column Address Hold Time	t _{CAH}	45	assable wa	55	1011/06/	ns	
Column Address Hold Time referenced to RAS	t _{AR}	95	+	120	- 1	ns	
Read Command Set-up Time	tRCS	0	+	0	- 1	ns	
Read Command Hold Time	tRCH	0		0	3W -	ns	
Write Command Hold Time	twcH	45	+	55		ns	
Write Command Hold Time referenced to RAS	twcr	95	-	120	-	ns	
Write Command Pulse Width	twp	45		55	- 810	ns	
Write Command to RAS Lead Time	t _{RWL}	45	_	55	-	ns	
Write Command to CAS Lead Time	tcwL	45	-	55	-	ns	
Data-in Set-up Time	tos	0	-	0	-	ns	9
Data-in Hold Time	t _{DH}	45	3 21764	55	M-GABA	ns	9
Data-in Hold Time referenced to RAS	t _{DHR}	95		120	-	ns	
CAS Precharge Time (for Page-mode Cycle Only)	tcP	60		80	-	ns	
Refresh Period	tref	- 12.45:	2	_	2	m s	
Write Command Set-up Time	twcs	-20		-20	-	ns	10
CAS to WE Delay	tcwp	60		80	999	ns	10
RAS to WE Delay	t _{RWD}	110		145	and the	ns	10
RAS Precharge to CAS Hold Time	trpc	0	+	0	-	ns	

NOTES

1. AC measurements assume $t_T = 5$ ns.

 8 cycles are required after power-on or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

 Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.

5. Assumes that $t_{RCD} \ge t_{RCD}$ (max).

6. Measured with a load circuit equivalent to 2TTL loads

 t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Operation with the t_{RCD} (max) limit insures that

 t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC} .

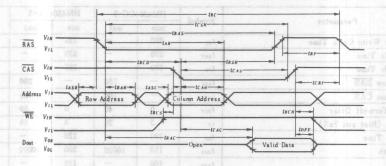
9. These parameters are reference to $\overline{\text{CAS}}$ leading edge in

 These parameters are reference to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.

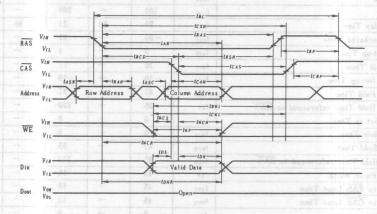
10. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERSMROVADVAW DRIMIT

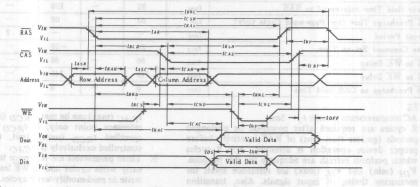
• READ CYCLE



• WRITE CYCLE

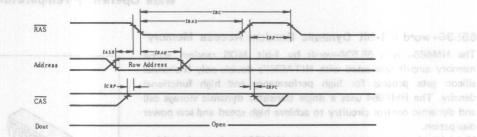


● READ-WRITE/READ-MODIFY-WRITE CYCLE

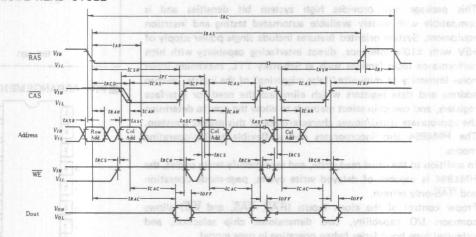


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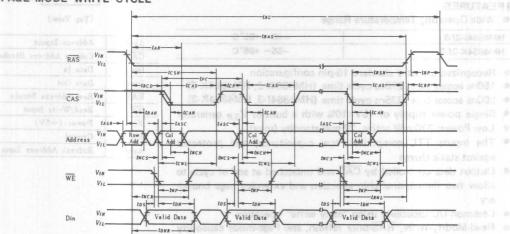
• "RAS-ONLY" REFRESH CYCLE



● PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



HM4864I-2, HM4864I-3, HM4864K-2, HM4864K-3

Wide Operating Temperature Range

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read, write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and RAS-only refresh.

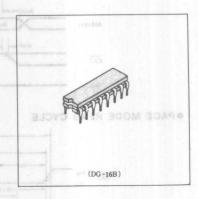
Proper control of the clock inputs (RAS, CAS, and WE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

FEATURES

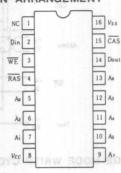
Wide Operating Temperature Range

HM48641-2/-3	−40~ +85°C			
HM4864K-2/-3	-55∼ +85°C			

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864I-2, HM4864K-2)
- 200ns access time, 335ns cycle time (HM4864I-3, HM4864K-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 22 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, and Page-mode capability
- 128 refresh cycle



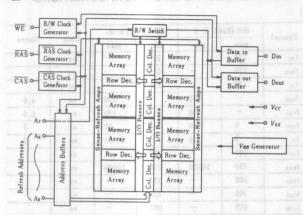
PIN ARRANGEMENT



(Top View)

A 0-A 7	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
A 0 - A 6	Refresh Address Input

FUNCTIONAL BLOCK DIARRACTERISTICS AND RECOMMENDE MARDAID BLOCK DIARRACTERISTICS.



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative

to V_{SS} -1.0 to +7V

Operating Temperature, Ta

(Ambient) . . -40 to +85°C (HM48641 Series)

-55 to +85°C (HM4864K Series)

Storage Temperature

(Ambient) -65 to +150°C

Short-circuit Output Current . 50 mA

Power Dissipation 1 W

RECOMMENDED DC OPERATING CONDITIONS $(Ta = -40 \text{ to } +85^{\circ}\text{C})^*$

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	Vcc Vcc	4.5	5.0	5.5	V	Leaster work
	Vss	0	0	0	V	Column Address
Input High Voltage	VIH	2.4	-	6.5	V V	orbit A 1 mula
Input Low Voltage	VIL VIL	-1.0	- 34	0.8	V	aubica 1 mulio

*: HM4864K Series; T_a = -55 to +85°C

DC ELECTRICAL CHARACTERISTICS ($T_a = -40 \text{ to } +85^{\circ}\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$, $V_{ss} = 0\text{V}$)

Parameter		Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling; t RC =	min.)	Icc1	o) beams:	60	m A	2,4
STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = V_{lik}$, Dout = High Impedance)	Jest Local	Iccz	smi smi	600 4 A	m A	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = V _{IH} ; t _{RC} = min.)	fac.	Iccs	-	45	m A	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation (RAS = V(L, CAS Cycling; tpc = min.)	loss.	Icc.	RAS consider Cyc	45	m A	2,4
INPUT LEAKAGE Input Leakage Current, any Input $(V_{i*} = 0 \text{ to } +6.5\text{ V}, \text{ all other pin}$ under test $= 0\text{ V}$)	s not	Iu	-10	10	μA	Write Co
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, Vost = 0 to +5.5V)	lare	ILO	-10	10	μА	BAS PER
OUTPUT LEVELS Output High (Logic 1) Voltage ($I_{out} = -5 \mathrm{mA}$) Output Low (Logic 0) Voltage ($I_{out} = 4.2 \mathrm{mA}$)		Voн Vol	2.4	V _{cc} 0.4	V remo Vese	CATO

NOTES

1. All voltages referenced to V_{SS} .

2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.

3. ILO consists of leakage current only.

4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

5. *: HM4864K Series; $T_a = -55$ to +85°C

■ AC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Ta=25°C)

ing too gish out her Parameter ties as a clove of	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-A7, Din)	Cini		7 333	pF	1
Input Capacitance (RAS, CAS, WE)	C 2		10	pF	001 bal
Output Capacitance (Dout) and the suggestion of	Cont	hich the out	te sinte at w	am pF Our	1,2

NOTES

1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable D_{OUT}.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS 13, 23

 $(Ta=-40 \text{ to } +85^{\circ}\text{C}^{*}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

Parameter	Symbol	HM4864I/K-2		HM 486	4I/K-3	Unit	Notes
Parameter	Symbol	min	max	min	max	Unit	Notes
Random Read or Write Cycle Time	t _{RC}	270	EUI Hos	335	Shoopy-	ns	NOT THE REAL
Read-Write Cycle Time	t _{RWC}	270		335	- 1	ns	187
Page Mode Cycle Time	t _{PC}	170		225	2000 902	ns	
Access Time from RAS	trac	_	150	and B	200	ns	4, 6
Access Time from CAS	tcac	-	100		135	ns	5, 6
Output Buffer Turn-off Delay	toff	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t _T	3	35	3	50	ns	3
RAS Precharge Time	t _{RP}	100	Ton	120	golf wat y	ns	
RAS Pulse Width	tras	150	10000	200	10000	ns	1/13
RAS Hold Time serrous (sand) time to the first	trsh	100	1	135	Harris II	ns	
CAS Pulse Width	tcas	100	lu <u>do</u> je:	135	- 1	ns	1001
CAS Hold Time	t _{CSH}	150		200	- 1	ns	
RAS to CAS Delay Time	tRCD	20	50	25	65	ns	8
CAS to RAS Precharge Time	tcrp	-20	-	-20	-	ns	-
Row Address Set-up Time	tasa	0	000076	0	757588	ns	
Row Address Hold Time	t _{RAH}	20	954	25	-	ns	W vlagu
Column Address Set-up Time	tasc	-5	64 -	-5		ns	
Column Address Hold Time	tCAH	45	204 -	55		ns	Sagra Maga
Column Address Hold Time referenced to RAS	t _{AR}	95	(4)4 =	120	- 1	ns	NOT END
Read Command Set-up Time	t _{RCS}	0	-	0	50 -	ns	# GB FRSEI
Read Command Hold Time	t _{RCH}	0	1110122	0	S. DEM	ns	1 24
Write Command Hold Time	twcn	45		55	- 1	ns	
Write Command Hold Time referenced to RAS	twcr	95	-	120	T 43	ns	TARES
Write Command Pulse Width	twp	45	AD, S. PA	55	Decay -	ns	Sasta
Write Command to RAS Lead Time	t _{RWL}	45	-	55	- 1	ns	SCINE!
Write Command to CAS Lead Time	tcwL	45	1000 - H	55	BRATTIN T SEG	ns	PE TERRO
Data-in Set-up Time	tos	0	-	0	- 1	ns	9
Data-in Hold Time	t _{DH}	45	-	55	B. 1.7	ns	9
Data-in Hold Time referenced to RAS	t _{DHR}	95	-	120	TV3	ns	OB ROL
CAS Precharge Time (for Page-mode Cycle Only)	tcP	60	Operation	80	as Carring	ns	112570
Refresh Period	tref	-	2	7,010	2	ms	GA7
Write Command Set-up Time	twcs	-10	/ 2 2 2 m	-10	- I	ns	10
CAS to WE Delay	tcwp	60	-	80	-	ns	10
RAS to WE Delay	t _{RWD}	110	_	145	- 1	ns	10
RAS Precharge to CAS Hold Time	trpc	0	or or A	hahinai 0 zi	and man	ns	e J tugie

NOTES

1. AC measurements assume $t_T = 5$ ns.

 8 cycles are required after power-on or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .

 Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.

5. Assumes that $t_{RCD} \ge t_{RCD}$ (max).

 Measured with a load circuit equivalent to 2TTL loads and 100 pF.

 t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Operation with the t_{RCD} (max) limit insures that

 t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC} .

 These parameters are reference to CAS leading edge in early write cycles and to WE leading edge in delayed

write or read-modify-write cycles.

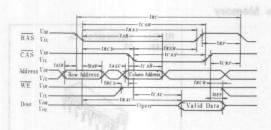
- 10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- 11. *: HM4864K Series; T₀ = -55 to +85°C

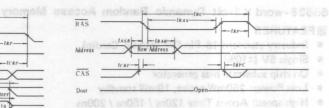


TIMING WAVEFORMS

• READ CYCLE

• "RAS-ONLY" REFRESH CYCLE

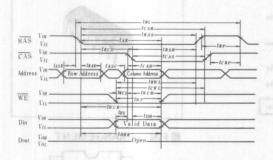


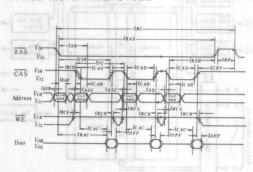


Page mode capability

• WRITE CYCLE

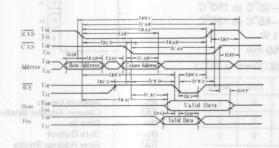
• PAGE MODE READ CYCLE

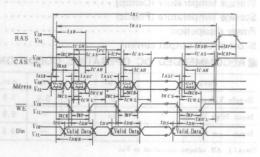




• READ-WRITE/READ-MODIFY-WRITE CYCLE

● PAGE MODE WRITE CYCLE





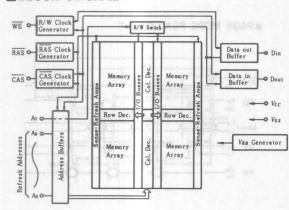
HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

65536-word × 1-bit Dynamic Random Access Memory

FEATURES

- Industry standard 16- Pin DIP (plastic, Cerdip)
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120ns / 150ns / 200ns
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by CAS
- TTL compatible
- 128 refresh cycles (2ms)
- Hidden refresh capability

■ BLOCK DIAGRAM



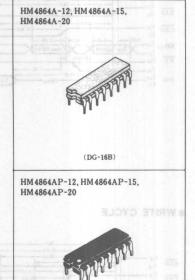
MASSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V _{SS} ······
Operating temperature, Ta (Ambient)0°C to 70°C
Storage temperature (Cerdip) · · · · · · · · · -65°C to 150°C
Storage temperature (Plastic) · · · · · · -55°C to 125°C
Power dissipation · · · · · · · · · · · · · · · · · · ·
Short circuit output current 50 mA

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	Vec	4.5	5.0	5.5	V	1
Input High Voltage	VIH	2.4		6.5	V	1
Input Low Voltage	VIL	-1.0	TE	0.8.	V	1

Notes: 1. All voltages referenced to Vss



PIN ARRANGEMENT



(Top View)

A0-A7	:	Address	Inputs

CAS : Column Address Strobe
Din : Data In
Dout : Data Output

 RAS
 : Row Address Strobe

 WE
 : Read/Write Input

 V_{CC}
 : Power (+5V)

V_{SS} : Ground A0-A6 : Refresh Address Inputs

DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±10%, Vss=0V)

atanyelete.	0 11	HM4864	HM4864A/P-12		HM4864A/P-15		HM4864A/P-20		Notes
Parameter	Symbol	min	max	min	max	min	ma x	Unit	Notes
Operating Current(RAS, CAS Cycling: tRC=min)	Icci	-	55	ino u en.	50	明护护	44	mA	1,2
Standby Cnrrent(RAS = VIH, Dout = High Impedance)	Iccz	sol-JT	3.5	Partie Li	3.5	0.20	3.5	mA	ALC: UK
Refresh Current(RAS Cycling, CAS = VIH, tRC = min)	Iccs	-	42	-	38	_	33	mA	2
Standby Current(RAS = VIH, Dout Enable)	Iccs	-	5.5	750	5.5	13500	5.5	mA	1
Page Mode Current(RAS = VIL, CAS Cycling; tPC = min)	Iccs	diam.	38		35	- C-1	31	mA	1,2
Input Leakage(0 < Vout < 6.5V)	ILI	-10	10	-10	10	-10	10	μΑ	100
Output Leakage(Dout is disabled, 0 < Vout < 5.5V)	ILO	-10	10	-10	10	-10	10	μA	6. 0
Output Levels High(I _{out} =-5mA)	Von	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	Series .
Output Levels Low(Iout-4.2mA)	VoL	0	0.4	0	0.4	0	0.4	V	017

Notes) 1. I_{cc} depends on output loading condition when the device is selected, I_{cc} max, is specified at the output open condition.

2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

CAPACITANCE ($V_{CC} = 5 \text{ V} \pm 10\%$, $T_{CC} = 25^{\circ}\text{C}$)

	Parameter	Symbol	typ	max	Unit	Notes
	A ₀ ~A ₇ , Din	Cial	-	5	pF	1
Input Capacitance	RAS, CAS, WE	Cin2		10	pF	1
Output Capacitance	Dout	Cout	-	7	pF	0 (1, 2)

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } 70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

D	CL.1	HM 48	864A-12	HM 4864A-15		HM 4864A -20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Note
Access Time From RAS	trac	-	120	-	150	-	200	ns	2, 3
Access Time From CAS	tcac	112	60	1717	75	_	100	ns	3, 4
Output Buffer Turn-off Delay	toff	100	35	X market	40	-	50	ns	5
Transition Time (Rise and Fall)	t _T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	t _{RC}	220	-	260	_	330	_	ns	
RAS Precharge Time	tRP	90	-	100	-	120	-	ns	
RAS Pulse Width	tras	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	tcas	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	tRCD	25	60	25	75	30	100	ns	7
RAS Hold Time	trsh	60	-	75	-	100	-	ns	
CAS Hold Time	tcsH	120	-	150	-	200	-	ns	
CAS to RAS Precharge Time	tcrp	-10	-	-10	-	-10	-	ns	
Row Address Set-up Time	tasa	0	-	0	-	0	-	ns	
Row Address Hold Time	t RAH	15	-	15	(STHE	20	AB) and	ns	MAY
Column Address Set-up Time	tasc	0	_	0	_	0	_	ns	
Column Address Hold Time	tcan	20	_	25	_	30	_	ns	
Column Address Hold Time Referenced to RAS	tar	80	_	100	-	130	-	ns	
WE Command Set-up Time	twcs	0		0	-	0	_	ns	8
Write Command Hold Time	twcH	40		45	-	55	-	ns	
Write Command Hold Time Referenced to RAS	twcr	100	1 -	120	_	155	-	ns	
Write Command Pulse Width	twp	40	-	45	_	55	-	ns	
Write Command to RAS Lead Time	t _{RW L}	40	- Tab	45	-	55	-	ns	1
Write Command to CAS Lead Time	tcwL	40	-4/-	45	-	55	-	ns	
Data-in Set-up Time	tos	0	1	0	A.	0	-	ns	9
Data-in Hold Time	t _{DH}	40		45	-	55	-	ns	9
Data-in Hold Time Referenced to RAS	tohr	100		120	-	155	_	ns	
Read Command Set-up Time	trcs	0	-/	0	_	0	-	ns	
Read Command Hold Time Referenced to CAS	t _{RCH}	0	1500	0	-	0	_	ns	
Read Command Hold Time Referenced to RAS	trrh	10	- 101 Pop-	10	-	10	-	ns	
Refresh Period	tref	Variet Date	2	-	2	_	2	ms	
Read-Write Cycle Time	t _{RWC}	245	(6)	280	-	345	-	ns	
CAS to WE Delay	tcwp	40		45	and the second	55	e -	ns	. 8
RAS to WE Delay	t _{RW D}	100	-	120	-	155	_	ns	
Page Mode Cycle Time	t _{PC}	120	-	145	-	190	_	ns	
CAS Precharge Time (for Page-mode Cycle Only)	tcp	50	-	60	-	80	-	ns	
CAS Precharge Time	tcpn	30	-	35	-	45	-	ns	
RAS Precharge to CAS Hold Time	trpc	0	_	0	_	0	_	ns	

HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

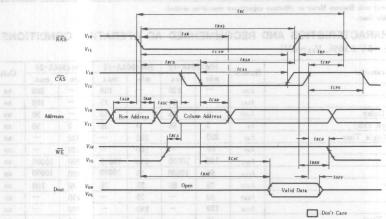
Notes

- 1. AC measurements assume $t_T = 5$ ns.
- Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
- t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- 7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .

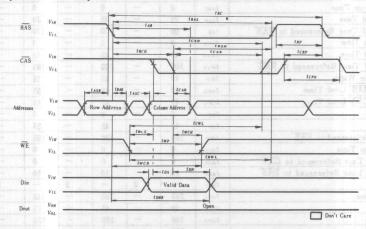
- t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
 - They are included in the data sheet is electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

TIMING WAVEFORMS

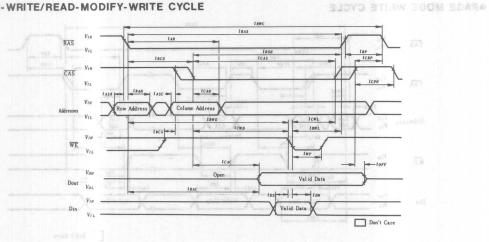
• READ CYCLE



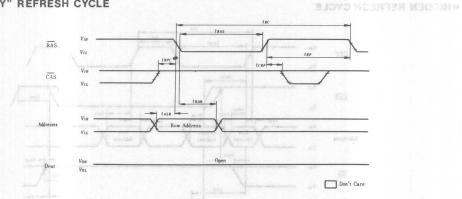
• WRITE CYCLE (EARLY WRITE)



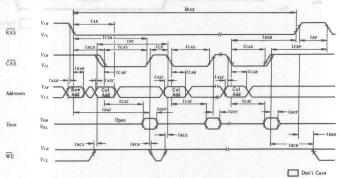
• READ-WRITE/READ-MODIFY-WRITE CYCLE



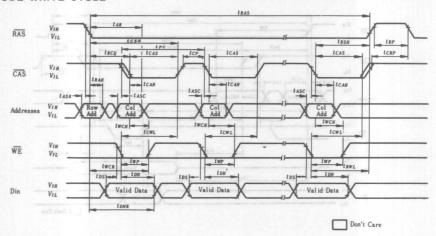
• "RAS-ONLY" REFRESH CYCLE



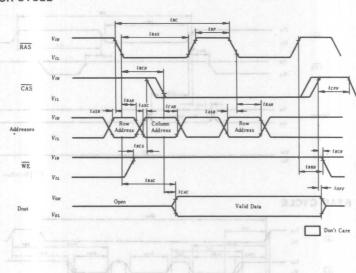
• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



•HIDDEN REFRESH CYCLE

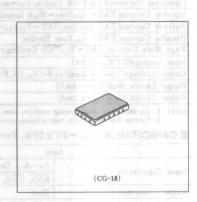


HM4864ACG-12, HM4864ACG-15, HM4864ACG-20 Preliminary

65536-word × 1-bit Dynamic Random Access Memory

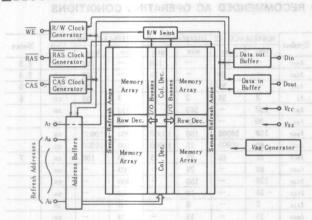
FEATURES

- 18-pin Leadless Chip Carrier
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120/150/200ns (max)
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by CAS
- TTL compatible
- 128 refresh cycles/2ms
- Hidden refresh capability



PIN ARRANGEMENT

■BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative t	o V _{SS}	1V to +7V
Operating temperature, Ta (Ambient)	0°C to +70°C
Storage temperature		65°C to +150°C
Power Dissipation		
Short circuit output current		

CAS V_{SS} NC Din 17 18 1 2 Dout 16 3 0 WE As 15 4 GRAS NC 114 5 0 NC As 12 7 Az

(Bottom View)

A0-A7 : Address Inputs
CAS : Column Address Strobe

Vss : Ground A0-A6 : Refresh Address Inputs

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Input High Voltage	VIH	2.4	1-	6.5	V	1
Input Low Voltage	VIL	-1.0		0.8	v	1

Notes: 1. All voltages referenced to Vss

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept, regarding specifications.

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±10%, Vss=0V)

	6 1 1	HM4864ACG-12		HM4864ACG-15		HM4864ACG-20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	ma x	Unit	Notes
Operating Current(RAS, CAS Cycling: tRC=min)	Icci	_	55	-	50	- T	44	mA	1,2
Standby Cnrrent(RAS - VIH, Dout - High Impedance)	Iccz	1295 73316	3.5	E (2313)	3.5	3200	3.5	mA	PUSPE
Refresh Current(RAS Cycling, CAS - VIH, tRC - min)	Iccs	-	42	-	38	_	33	mA	2
Standby Current(RAS - VIH, Dout Enable)	Iccs	-	5.5	-	5.5	Digitis C	5.5	mA	.81
Page Mode Current(RAS = VIL, CAS Cycling; tpc = min)	Icce	-	38	-	35	- /	31	mA	1,2
Input Leakage(0 < Vout < 6.5V)	ILI	-10	10	-10	10	-10	10	μΑ	-
Output Leakage(Dout is disabled, 0 < Vout < 5.5V)	ILO	-10	10	-10	10	-10	10	μA_	1350
Output Levels High(Iout=-5mA)	Von	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	102
Output Levels Low(Iout=4.2mA)	Vol	0	0.4	0	0.4	0	0.4	V	PH I

Notes) 1. Icc depends on output loading condition when the device is selected, Icc max. is specified at the output open condition.

2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

EXAMPLE 10% CAPACITANCE $(V_{cc}=5V\pm10\%, Ta=25^{\circ}C)$

	Item	Symbol	typ	max	Unit	Notes
Input Capacitance	Cin1	-	5	pF	101	
Input Capacitance	RAS, CAS, WE	Cinz	-	10	pF	1
Output Capacitance	Dout	Cout	-	7	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} - V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } 70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

Peremeter	Symbol	HM4864	ACG-12	HM4864	IACG-15	HM4864	ACG-20	Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Onit	Notes
Access Time From RAS	trac	40	120	_	150	-	200	ns	2, 3
Access Time From CAS	tcac	-	60	1 -	75	-	100	ns	3, 4
Output Buffer Turn-off Delay	toff	-	35	VAT2	40	Acres	50	ns	5
Transition Time (Rise and Fall)	t _T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	tRC	220	-	260	M F	330	-	ns	
RAS Precharge Time	trp	90	-	100	附出	120		ns	
RAS Pulse Width	tras	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	tcas	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	tRCD	25	60	25	75	30	100	ns	7
RAS Hold Time	trsh	60	-	75	1 10+1	100	-	ns	
CAS Hold Time	tcsH	120	-	150	11+1	200	-	ns	
CAS to RAS Precharge Time	tcrp	-10	-	-10	للبراء	-10		ns	
Row Address Set-up Time	task	0	-	0	15-0	0		ns	
Row Address Hold Time	trah	15	-	15	-	20	-	ns	
Column Address Set-up Time	tasc	0	-	0	ATTAR	0	XAR	ns	ABSI
Column Address Hold Time	tCAH	20	-	25	- 17	30	or sie	ns	marta
Column Address Hold Time Referenced to RAS	tar	80	-	100	66-	130	-	ns	
WE Command Set-up Time	twcs	0	1014	0	T COLUMN TO A	0	11414	ns	8
Write Command Hold Time	twch	40	-	45		55	61.428	ns	SPETO
Write Command Hold Time Referenced to RAS	twcn	100		120		155	170	ns	1 19160
Write Command Pulse Width	twp	40	-	45	-	55	o man	ns	in tune
Write Command to RAS Lead Time	t RW L	40	-	45	-	55	-	ns	
Write Command to CAS Lead Time	tcwl	40	-	45	-	55	-	ns	
Data-in Set-up Time	tos	0	_	0		0		ns	9
Data-in Hold Time	t _{DH}	40	1 7 153803	45	1/5/24	55	1-0.03.48	ns	9
Data-in Hold Time Referenced to RAS	tohr	100	1 -	120	-	155	-	ns	
Read Command Set-up Time	tres	0	1 - 2	0		0		ns	on the later of
Read Command Hold Time Referenced to CAS	t RCH	0	1 10	0	-20	0	-	ns	X (992)
Read Command Hold Time Referenced to RAS	trrh	10	-	10	-	10		ns	Ell Susav
Refresh Period	tref	-	2	-	2	+	2	ms	7
Read-Write Cycle Time	t RW C	245	-	280	1 -	345		ns	100 mg
CAS to WE Delay	tcw p	40	_	45	-	55	pia 112 11 a	ns	8
RAS to WE Delay	t _{RW D}	100	-	120	-	155	- 1	ns	
Page Mode Cycle Time	t _{PC}	120	Stiph House	145	- troder	190	84C) (77 940	ns	361 190
CAS Precharge Time (for Page-mode Cycle Only)	tcp	50	HISTORY MAN	60	1000	80	2017	ns	1000
CAS Precharge Time	tcpn	30	-	35	-	45	_	ns	
RAS Precharge to CAS Hold Time	trpc	0	-	0	_	0	_	ns	

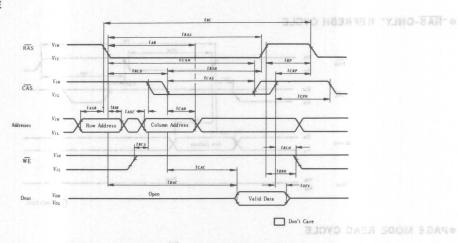
Notes

- 1. AC measurements assume $t_T = 5$ ns.
- Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- 3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that $t_{RCD} \ge t_{RCD}$ (max). 5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- 7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by tCAC.

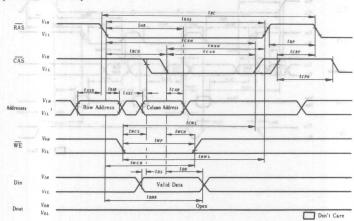
- 8. twcs, tcwD and tRwD are not restrictive operating parameters.
 - They are included in the data sheet is electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- 9. There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- An initial pause of 100 µs is required after power-up followed by a minimum of 8 initialization cycles.

TIMING WAVEFORMS

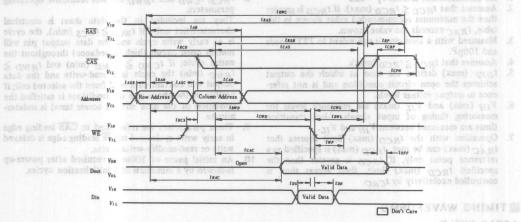
• READ CYCLE



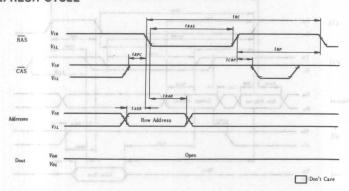
• WRITE CYCLE (EARLY WRITE)



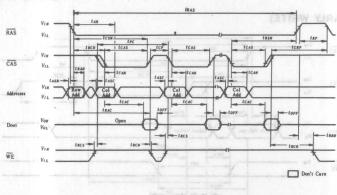
• READ-WRITE/READ-MODIFY-WRITE CYCLE



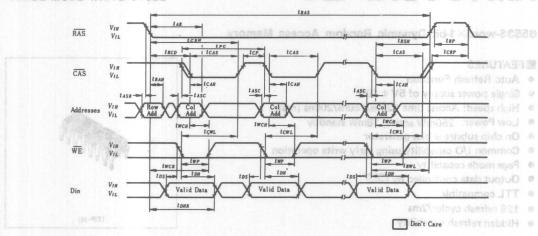
•"RAS-ONLY" REFRESH CYCLE



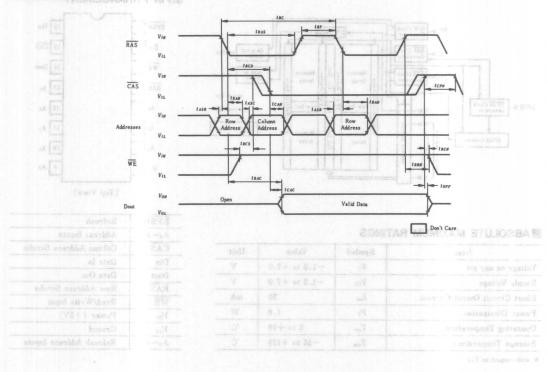
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



HIDDEN REFRESH CYCLE



THE COMMENDED DO OPERATING CONDITIONS (X = 0 to + 70°C)

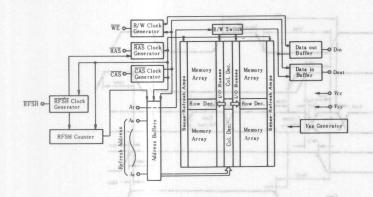
HM4865AP-12, HM4865AP-15*HM4865AP-20

65536-word×1-bit Dynamic Random Access Memory

FEATURES

- Auto Refresh Function
- Single power supply of 5V ± 10%
- High speed: Access time 120ns/150ns/200ns (max.)
- Low Power: 250mW active, 18mW standby
- On chip substrate bias generator
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by CAS
- TTL compatible
- 128 refresh cycles/2ms
- Hidden refresh capability

BLOCK DIAGRAM



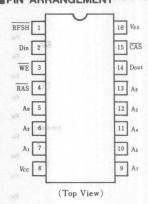
MADE ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin	V_T	-1.0 to +7.0	V
Supply Voltage	Vcc	-1.0 to +7.0	V
Short Circuit Output Current	Iout	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	Tate	-55 to +125	°C

^{*} with respect to Vss

(DP-16)

PIN ARRANGEMENT



RFSH	Refresh
A ₀ ~A ₇	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
A0~A6	Refresh Address Inputs

RECOMMENDED DC OPERATING CONDITIONS $(Ta=0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	V_{ss}	0	0	0	V
Input Voltage	V_{IH}	2.4		6.5	V
	V_{IL}	-1.0		0.8	V

Note) All voltages referenced to Vss.

DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, $V_{cc}=5V\pm10\%$, $V_{ss}=0V$)

Charles Anna Assar Anna Anna	6 11	HM4865	A/P-12	HM4865	A/P-15	HM4865	A/P-20	Unit	Notes
Parameter	Symbol	min	max	min	max	min	ma x	Cilit	Notes
Operating Current(RAS, CAS Cycling: tRC = min)	Icci	20.7	55	_	50	-	44	mA	1,2
Standby Cnrrent(RAS = V _{IH} , Dout = High Impedance)	Iccz	-	3.5		3.5	-	3.5	mA	17
Refresh Current(RAS Cycling, CAS = VIH, tRC = min)	Iccs	1	42		38		33	mA	2
Standby Current(RAS = VIH, Dout Enable)	Iccs	sya1	5.5	-	5.5	110 <u>26</u> 61	5.5	mA	1
Page Mode Current(RAS = V _{IL} , CAS Cycling; t _{PC} = min)	Icc6	107	38	O HOY	35	ME'T'S	31	mA	1,2
Auto Refresh Current ($\overline{RFSH} = Cycle, \overline{RAS} = V_{IH}$)	Icci	10.00	44	-	40	_	35	mA	entrolle G
Input Leakage(0 < Vout < 6.5V)	ILI	-10	10	-10	10	-10	10	μA	1
Output Leakage(Dout is disabled, 0 < Vout < 5.5V)	ILO	-10	10	-10	10	-10	10	μA	0.000.00
Output Levels High(Iout = -5mA)	VoH	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	E BAO
Output Levels Low(Iout=4.2mA)	Vol	0	0.4	0	0.4	0	0.4	V	RASIN

Notes) 1. Icc depends on output loading condition when the device is selected, Icc max. is specified at the output open condition.

2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

CAPACITANCE $(V_{CC}=5V\pm10\%, Ta=25^{\circ}C)$

	Parameter	Symbol	typ	max	Unit	Notes
	A ₀ ~A ₇ , Din	Cin1		5	pF	1
Input Capacitance	RAS, CAS, WE	Cin2		10	pF	1
Output Capacitance	Dout	Cout		7	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS $(Ta=0 \text{ to } 70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

AC CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $V_{ss}=0V$, $T_a=0$ to $+70^{\circ}$ C)^{13,23}(20m), $V_{ss}=0$ (almost $V_{ss}=0$)

alcat sids ni nwode acii pies a moses manitant	Symbol	HM486	5AP-12	HM486	5AP-15	HM486	5AP-20	U.A.	Notes
Item	Symbol	min	max	min	max	min	max	Unit	Notes
Random Read or Write Cycle Time	t _{RC}	220		260	(a)(1.78)	330	ra sa a o m	ns	
Read-Write Cycle Time	t RWC	245	s saffat	280	omit of	345	(20070)	ns	
Page Mode Cycle Time	t _{PC}	120	-	145		190	istle - k u	ns	
Access Time from RAS	t RAC	gra t <u>m</u> it	120	zlasi <u>l</u> (x	150	t edi_da	200	ns	4, 6
Access Time from CAS	tCAC	SET MOST	60	District to	75	COMP.	100	ns	5, 6
Output Buffer Turn-off Delay	t off	ghe ge il	35	of This	40	153 875 15	50	ns	7
Transition Time(Rise and Fall)	t _T	3	35	3	35	3	50	ns	3
RAS Precharge Time	t _{RP}	90	Do edito	100	A 028 G	120	CHOIL 4	ns	
RAS Pulse Width	tras	120	10000	150	10000	200	10000	ns	
RAS Hold Time	t _{RSH}	60	Luano- 0	75	uo s a al	100	s so le s	ns	
CAS Pulse Width	tcas	60	10000	75	10000	100	10000	ns	
CAS Hold Time	t _{CSH}	120		150	-	200	_	ns	
RAS to CAS Delay Time	t RCD	25	60	25	75	30	100	ns	8
CAS to RAS Precharge Time	t _{CRP}	-10		-10		-10	-	ns	
Row Address Set-up Time	task	0		0	_	0	-	ns	
Row Address Hold Time	t RAH	15	_	15	_	20	_	ns	
Column Address Set-up Time	tasc	0	-	0		0	_	ns	
Column Address Hold Time	t CAH	20	-	25		30	-	ns	
Column Address Hold Time referenced to RAS	tAR	80	_	100		130	_	ns	
Read Command Set-up Time	t _{RCS}	0	=	0	-	0	-	ns	
Read Command Hold Time	t _{RCH}	0		0	_	0	-	ns	
Write Command Hold Time	t wcH	40		45		55	_	ns	
Write Command Hold Time referenced to RAS	twcr	100	-	120	_	155	_	ns	
Write Command Pulse Width	t wp	40	-	45	-	55	-	ns	
Write Command to RAS Lead Time	t RWL	40	-	45	-	55	_	ns	

(to be continued)

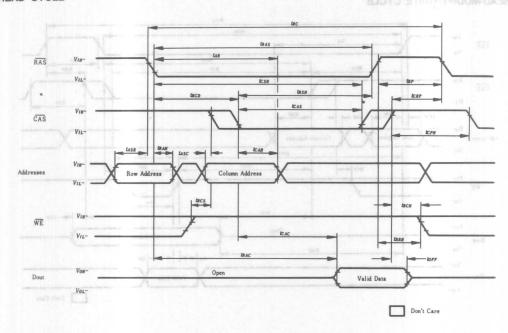


Item V * seV .WOT ± V2-	0 11	HM486	5AP-12	HM486	5AP-15	HM486	5AP-20	***	Notes
Item V = 22 V AVOI ± V2-	Symbol	min	max	min	max	min	ınax	Unit	
Write Command to CAS Lead Time	t cwl	40	_	45	-	55	4 -	ns	
Data-in Set-up Time	tos	0	_	0	oalt en ile	0	₹ ASLue	ns	9
Data-in Hold Time	t DH	40		45	M Agree	55		ns	9
Data-in Hold Time referenced to RAS	toHR	100	-	120	told and	155	+SER	ns	v:lbma18
CAS Precharge Time(for Page-mode Cycle Only)	tcp	50	(Alm	60	Ing3_8	80	77.51 1. ra	ns	1/ 1/21/9
Refresh Period	tref	Lecz	2	(10 mg	2	3− T Sc	2	ns	Auto Re
Write Command Set-up Time	twcs	0	-	0	S V 0	0	C. T. SHARE	ns	10
CAS to WE Delay	tcwD	40	-	45	-	55	- Jwgii	ns	10
RAS to WE Delay	t RWD	100		120		155	Tie V ile a	ns	negrac
RAS Precharge to CAS Hold Time	t RPC	0	ha ici <u>soiv</u>	0	a nextilizad	0	oppo es es	ns	. Canh
Read-modify-write Hold Time	t _{RRH}	10	1-	10	Xonz -	10	7 700	ns	V 2 M 1
CAS Precharge Time	tcpn	30	_	35	100	45	-	ns	
RFSH Set-up Time	tFSR	90		100	19900	120		ns	
RAS to RFSH Delay Time	t _{RFD}	90		100	200 50	120	- 9	ns	D togo
RFSH Cycle Time	t FC	220	-	260	-	330	850	ns	100301
RFSH Pulse Width	t _{FP}	120	5000	150	5000	200	5000	ns	f (sate
RFSH Precharge Time	t _{FI}	90	_	100	_	120	Santair v	ns	2

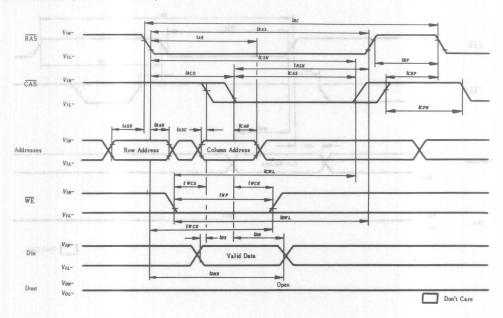
Notes) 1. AC measurements assume $t_T = 5ns$.

- 2. An initial pause of 100 µs is required after power-up followed by a minimum of 8 initalization of cycles.
- 3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Assumes that t_{RCD} = t_{RCD}(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- 5. Assumes that t_{RCD}=t_{RCD}(max).
- 6. Measured with a load circuit equivalent to 2TTL loads and 100pF.
- t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD} (max) is specified as a reference
 point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by
 t_{CAC}.
- 9. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
- 10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} = t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} = t_{CWD}(min) and t_{RWD}(min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

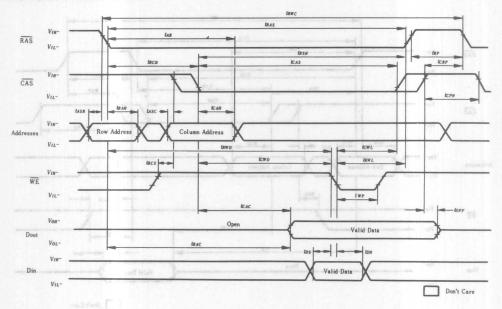
■ TIMING WAVEFORM • READ CYCLE



• WRITE CYCLE (EARLY WRITE)

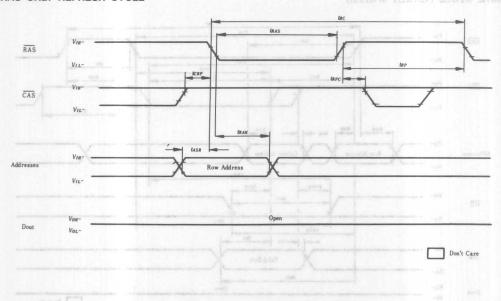


• READ-MODIFY-WRITE CYCLE



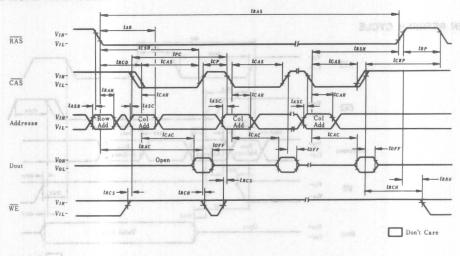
BETWING WAVEFORM

• RAS ONLY REFRESH CYCLE

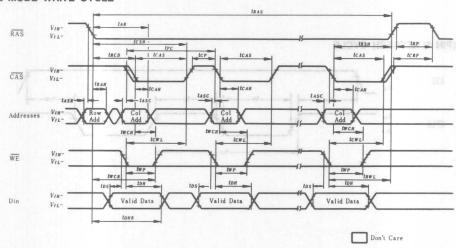


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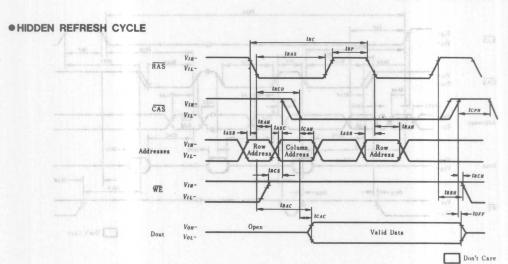
• PAGE MODE READ CYCLE



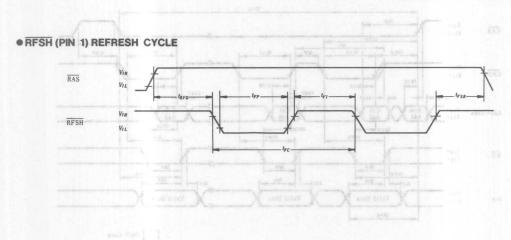
• PAGE MODE WRITE CYCLE



PRAGE MODE READ CYCLE



OPAGE MODE WRITE CYCLE



HM50256-12, HM50256-15 Preliminary HM50256-20

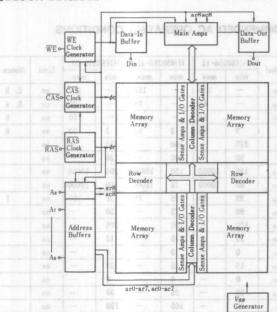
262144-word × 1-bit Dynamic Random Access Memory

FEATURES

- Industry Standard 16-Pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 23mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles/4ns
- 3 variation of refresh . . . RAS only refresh

CAS before RAS refresh Hidden refresh

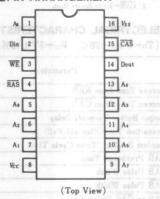
BLOCK DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to VSS	 	 1V to +7V
Operating temperature, Ta (Ambient)	 	 0°C to +70°C
Storage temperature	 	-65°C to +150°C
Power dissipation	 	 . 08 1W
Short circuit output current	 	 50mA

PIN ARRANGEMENT



$A_0 \sim A_8$	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
V_{ss}	Ground
A0~A7	Refresh Address Inputs

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales Dept, regarding specifications.

RECOMMENDED DC OPERATING CONDITIONS $(Ta=0 \text{ to } +70^{\circ}\text{C})$

Parameter	Symbol	min and	typ	max	Unit	Note
Supply Voltage	Vcc	4.5	5.0	5.5	V	bigamin 1 bas)
Input High Voltage	V _{IH}	2.4	_	6.5	V block	basmad I hee
Input Low Voltage	V _{IL}	-1.0		0.8	V	breign 1 han)

Note) 1. All voltages referenced to Vss

DC ELECTRICAL CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm10\%$, $V_{ss}=0V$)

	0 11	HM50	256-12	HM50256-15		HM50256-20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Operating Current(RAS, CAS Cycling: tRC=min)	Icci	caeno	83	bnszi	70	SWCT N	55	mA	1
Standby Current(RAS = VIH, Dout = High Impedance)	Iccz	-	4.5	-	4.5	-	4.5	mA	
Refresh Current(RAS only Refresh, tRC=min)	Tocs	_	62	_	53	_	42	mA	FARR
Standby Current(RAS = VIH, Dout Enable)	Iccs	_	10	-	10	10-01-	10	mA	1
Refresh Current(CAS before RAS Refresh, tRC=min)	I _{CC6}	-	69	_	58	B 1 1	45	mA	100000
Input leakage(0 < Vout < 7V)	Iu	-10	10	-10	10	-10	10	μА	Unio
Output leakage(0 < Vout < 7V)	ILO	-10	10	-10	10	-10	10	μΑ	The state of
Output levels High(Ioni = -5mA)	V_{OH}	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	110.1
Output levels Low(Iout-4.2mA)	Vol	0	0.4	0	0.4	0	0.4	V	138 11

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

CAPACITANCE ($V_{cc}=5V\pm10\%$, $Ta=25^{\circ}C$)

P	arameter	Symbol	typ	max	Unit	Notes
(Bit-00)	Address, Data-in	des Cn 1 0	Defore R.	amisa PAO 5	1	
Input Capacitance	Clocks, Data-out	Cn	len r ef iresh	7	pr	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS - VIH to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, \ V_{cc}=5\text{V}\pm10\%, \ V_{ss}=0\text{V})$

	1	******	000 00	TTREE	050 15	777450	050 00		
Parameter	Symbol		256-12		256-15	10000000	256-20	Unit	Notes
The latest the second s		min	max	min	max	min	max		
Access Time from RAS	t RAC	-	120	121	150		200	ns	2, 3
Access Time from CAS	tcac	_	60	Het-	75	_	100	ns	3, 4
Output Buffer Turn-off Delay	toff	gr ou nd)	30	515-	40	-	50	ns	5
Transition Time(Rise and Fall)	t _T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t RC	220	8	260	-	330	2 A F. S.	ns	
RAS Precharge Time	t _{RP}	90		100	_	120	Care and	ns	
RAS Pulse Width	tras	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	tcas	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	t RCD	25	60	25	75	30	100	ns	7
RAS Hold Time	t RSH	60		75	-	100	1 -	ns	
CAS Hold Time	t csh	120	10	150	ements.	200	souther.	ns	
CAS to RAS Precharge Time	t _{CRP}	10	10	10	80513	10	47 16 MILE I	ns	
Row Address Set-up Time	task	0	15	0	-	0	-	ns	
Row Address Hold Time	t RAH	15	100	15	-	20	-	ns	
Column Address Set-up Time	tasc	0	-	0		0	-	ns	1106
Column Address Hold Time	t CAH	20	-	25	396,375,000	30	-	ns	
Column Address Hold Time referenced to RAS	t _{AR}	80	-	100	-	130	_	ns	
WE Command Set-up Time	twcs	0	_	0	MITES	0	EXAM	ns	1008
Write Command Hold Time	twch	40		45	29 V 01	55	n ni a i	ns	aparti
Write Command Hold Time referenced to RAS	twcs	100	-	120	pidrus.	155	1176100	ns	Fransi
Write Command Pulse Width	twp	40_	-	45	-	55	10711757	ns	BESSIE
Write Command to RAS Lead Time	t RWL	40	-	45	-	55	-	ns	1910
Write Command to CAS Lead Time	t CWL	40	-	45	-	55	5 	ns .	A. 1723
Data-in Set-up Time	tos	0	-	0	-	0	_	ns	9
Data-in Hold Time (DOV+	t DH	40	11040	45	73,929	55	(34)	ns	8, 9
Data-in Hold Time referenced to RAS	t DHR	100	loi e	120	-	155	_	ns	
Read Command Set-up Time	trcs	0	1000	0	_	0	-	ns	
Read Command Hold Time referenced to CAS	t RCH	0	-	0	-	0	_	ns	7150
Read Command Hold Time referenced to RAS	t RRH	10	-	10	-	10	_	ns	1
Refresh Period	tref		4		4		4	ms	200

(to be continued)

Rage mode capability
 TL compatible

256 refresh cycles 4ns

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
rarameter	Symbol	min	max	min	max	min	max	Unit	Notes
Read-Write Cycle Time	t RWC	265		310	_	390	_	ns	
CAS to WE Delay	t cwp	60	-	75		100		ns	8
RAS to WE Delay	t RWD	120	range on	150		200	<u>C.2008</u>	ns	
CAS Precharge Time	t _{CPN}	50	-	60		80	_	ns	
CAS Setup Time	tcsr	. 10	7	10	-	10	_	ns	
CAS Hold Time (CAS before RAS Refresh)	t CHR	120	-	150	-	200	_	ns	
RAS Precharge to CAS Hold Time	t RPC	0	×	0	-	0	_	ns	

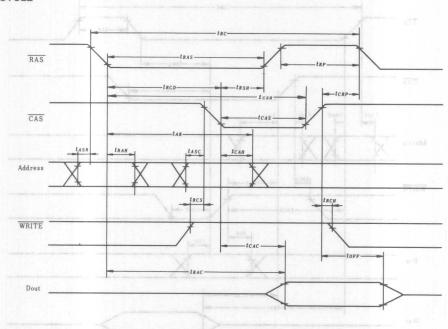
Notes

- 1. AC measurements assume $t_T = 5$ ns.
- 2. Assumes that $t_{RCD} \le t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
- t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- 7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .

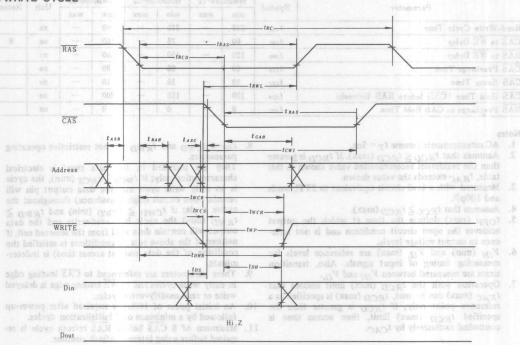
- t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
- They are included in the data sheet is electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- 10. An initial pause of 100µs is required after power-up followed by a minimum of 8 initialization cycles.
- 11. Minimum of 8 CAS before RAS refresh cycle is required before using internal refresh counter.

TIMING WAVEFORMS

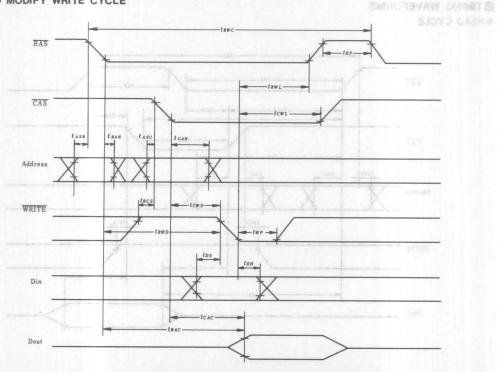
• READ CYCLE



• WRITE CYCLE

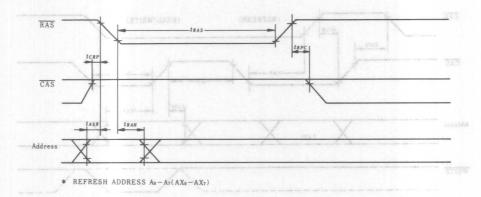


• READ MODIFY WRITE CYCLE

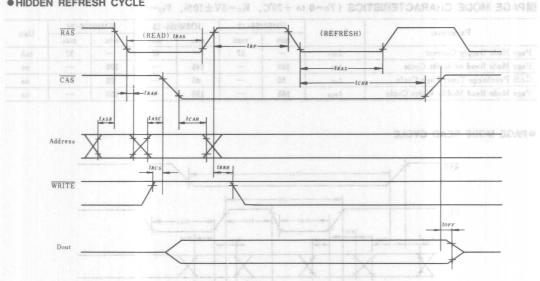


*COUNTER TEST

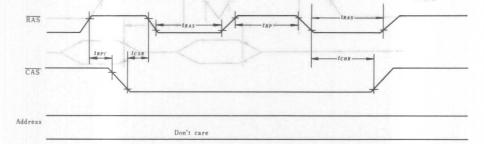
• RAS ONLY REFRESH CYCLE



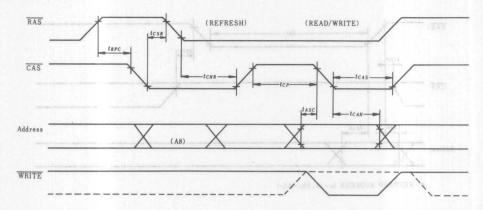
• HIDDEN REFRESH CYCLE



• CAS BEFORE RAS REFRESH CYCLE



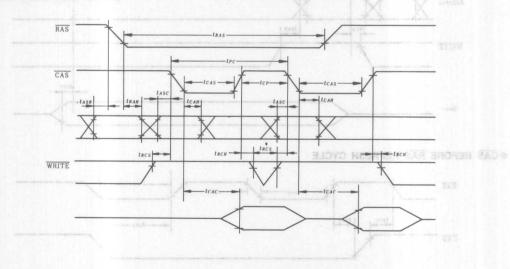
• COUNTER TEST



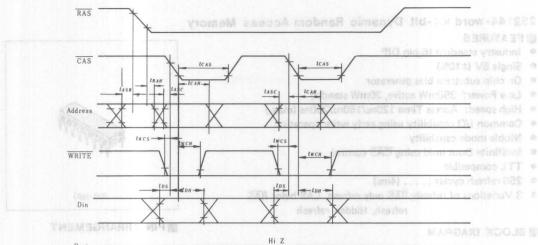
■PAGE MODE CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5$ V $\pm 10\%$, $V_{ss}=0$ V)

Parameter	Symbol HM50256-12		256-12	HM50	256-15	HM50	Unit	
	Symbol	min	max	min	max	min	max	Unit
Page Mode Supply Current	Icci	1 -	57	1 1-	48	1 -	37	mA
Page Mode Read or Write Cycle	t _{PC}	120	-	145		190	-	ns
CAS Precharge Time, Page Cycle	tcp	50	-	60	1	80	22.0	ns
Page Mode Read Modify Write Cycle	t PCM	165	-	195		250	_	ns

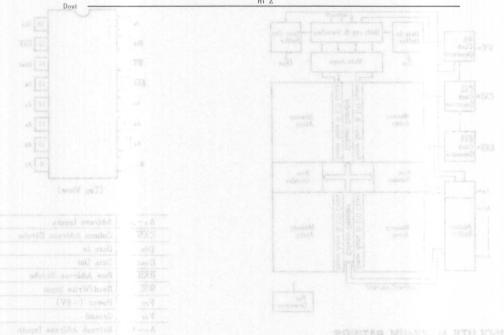
• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



To the second transfer of the second transfer

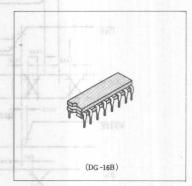


HM50257-12, HM50257-15, Preliminary HM50257-20

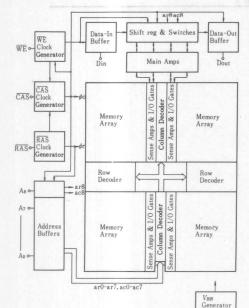
262144-word × 1-bit Dynamic Random Access Memory

FEATURES

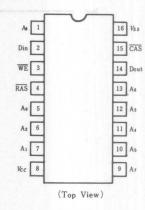
- Industry standard 16-pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- Indifinite Dout hold using CAS control
- TTL compatible
- 256 refresh cycles (4ms)
- 3 Variations of refresh; RAS only refresh, CAS befor RAS refresh, Hidden refresh



BLOCK DIAGRAM



■ PIN ARRANGEMENT



A 0~A8	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
V_{ss}	Ground
A0~A7	Refresh Address Inputs

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to	to V _{SS} 1V to +7V	1
Operating temperature, Ta (A	(Ambient) 0°C to +70°C	,
Storage temperature	65°C to +150°C	,
Power dissipation		1
Short circuit output current	t	

RECOMMENDED DC OPERATING CONDITIONS $(T_a=0 \text{ to } +70 \text{ }^{\circ}\text{C})$

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Input High Voltage	VIH	2.4	-	6.5	V	1
Input Low Voltage	VIL	-1.0	_	0.8	V	1

Note 1) All voltages referenced to Vss.

The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales

Dept, regarding specifications.

DC ELECTRICAL CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm10\%$, $V_{ss}=0V$)

man min and man man	C 1 1	HM50	257-12	HM50	257-15	HM50	257-20	Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Operating Current (RAS, CAS Cycling: tRC=min)	Icci	awo l	83	-	70	_	55	mA	810
Stand by Current (RAS = VIH, Dout = High Impedance)		See 1	4.5	_	4.5	-	4.5	mA	LAR
Refresh Current (RAS only Refresh, tRC=min)		5-1 -	62	_	53	-	42	mA	CAS Y
Standby Current ($\overline{RAS} = V_{IH}$, Dout Enable)		88.03	10	_	10	-	10	mA	210
Refresh Current (CAS before RAS Refresh, tRC=min)	Icc 6	A WD T	69	(d ee))	58	900 00 0	45	mA	H F AD
Input leakage (0 < Voit < 7V)	I_{LI}	-10	10	-10	10	-10	10	μΑ	1 8 1
Output leakage (0 < Vout < 7V)	ILO	-10	10	-10	10	-10	10	μA	
Output levels High (Iout = -5 mA)	Von	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	E5. (0)K
Output levels Low (Iout=4.2mA)	Vol	0	0.4	0	0.4	0	0.4	V	2 4

Notes) 1. Icc depends on output loading condition when the device is selected Icc max, is specified at the output open condition.

■ CAPACITANCE (Vcc=5V±10%, Ta=25°C)

S owest bas (sim) ovePa	Symbol	typ	max	Unit	Notes		
Input Capacitance	Address, Data-In	Cri ad	ficials it a	5	ffei (zmm)	3801	
	Clocks, Data-Out	C12	pera Rouse	7	property and	1, 2	

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS-V_{III} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$

wed by a minimus of Kimitiglization cycles.	Symbol	HM50	257-12	HM50	257-15	HM50	257-20	Unit	Notes
Parameter	Symbol	min	max	min	max	min	max		
Access Time from RAS		-	120	-	150	-	200	ns	2,3
Access Time from CAS	tcac	_	60	-	75	-	100	ns	3,4
Output Buffer Turn-off Delay	toff	_	30	_	40	MAO	50	ns	5
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	tRC	220	-	260	-	330		ns	
RAS Precharge Time	tRP	90	-	100	-	120	_	ns	
RAS Pulse Width	tras	120	10000	150	10000	200	10000	ns	
RAS Pulse Width	tcas	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	tRCD	25	60	25	75	30	100	ns	7
RAS Hold Time	trsh	60	_	75		100	-	ns	
CAS Hold Time	tcsH	120		150		200	-	ns	
CAS to RAS Precharge Time	tcrp	10	_	10	-	10	_	ns	
Row Address Set-up Time	tASR	0	_	0	-	0	5 <u>AB</u> -	ns	
Row Address Hold Time	trah	15	11.1	15		20	_	ns	
Column Address Set-up Time	tasc	0	-	0	2 -	0	-1	ns	
Column Address Hold Time	tcan	20		25		30		ns	
Column Address Hold Time referenced to RAS	tAR	80	X -	100	-	130	_	ns	
WE Command Set-up Time	twcs	0	-	0	-	0	-	ns	8
Write Command Hold Time	twcH	40	-	45	-	55	_	ns	
Write Command Hold Time referenced to RAS	twcr	100	-	120	-	155		ns	
Write Command Pulse Width	twp	40	-	45	-	55	3,718	ns	
Write Command to RAS Lead Time	tRWL	40	1-	45		55		ns	
Write Command to CAS Lead Time	tcwl	40	-	45	-	-55	,—,	ns	
Data-in Set-up Time	tos	0	-	0 -	-	0	_	ns	9
Data-in Hold Time	t _{DH}	40	10° 1-1	45	-	55		ns	8,9
Data-in Hold Time referenced to RAS	t _{DHR}	100	_	120	-	155	-	ns	
Read Command Set-up Time	trcs	0		0	-	0	_	ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0	_	0	_	0	_	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	_	10	-	10	_	ns	
Refresh Period	tREF	_	4	-	4	_	4	ns	

(to be continued)



7144-851	C 11	HM50257-12	HM50257-15		HM50257-20		17.1	N.				
Parameter		Symbol	min	min max	min	max	min	max	Unit	Notes		
Read-Write Cycle Time	768	s site	ALFORE.	trwc	265	_	310	_	390	_	ns	
CAS to WE Delay	- 177		88	tcwp	60	- to le	75	mila -	100	(38) 24 6	ns	8
RAS to WE Delay	- 114	90	Bak	tRWD	120	(01 18)	150	H-1-0	200	(A)) to	ns	Stand P
CAS Precharge Time	- 1 18		20	tcpn	50	-	60	r "dz — ti	80	SAN-u	ns	Robessi
CAS Setup Time	- 100	-	-01	tcsR	10	-	10	lecil o	10	EAR-W	ns	Standly
CAS Hold Time (CAS be	fore RAS	Refresh)	éd	tchr	120	(gim—g	150	es and	200	8.63	ns	efres
RAS Precharge-to CAS	Hold Time	01-	0.5	tRPC	0	-	0	-	0	140/03	ns	Inqui

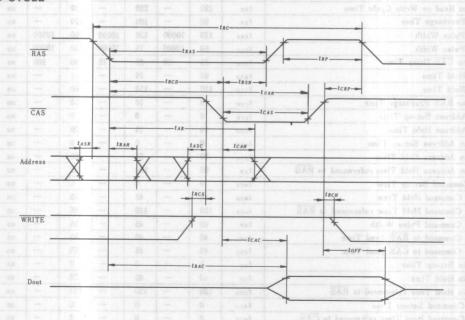
Notes

- 1. AC measurements assume $t_T = 5$ ns.
- 2. Assumes that $t_{RCD} \le t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
- t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- 7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .

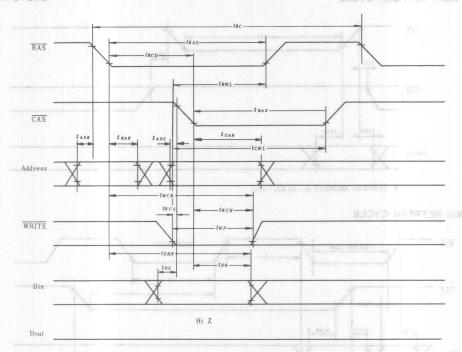
- t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
 - They are included in the data sheet as electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization cycles.
- Minimum of 8 CAS before RAS refresh cycle is required before using internal refresh counter.

TIMING WAVEFORMS

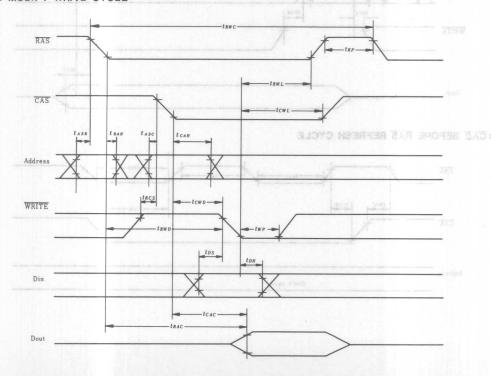
• READ CYCLE



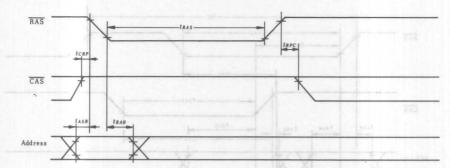
• WRITE CYCLE



• READ MODIFY WRITE CYCLE

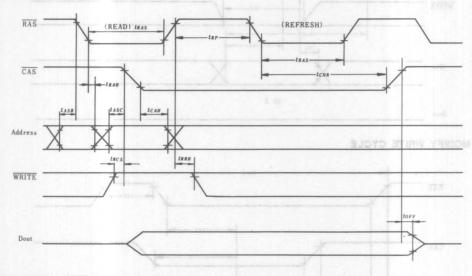


• RAS ONLY REFRESH CYCLE

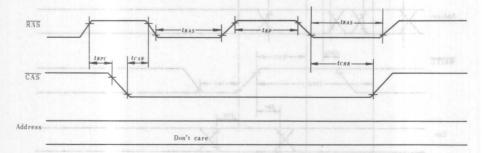


* REFRESH ADDRESS A0-A7(AX0-AX7)

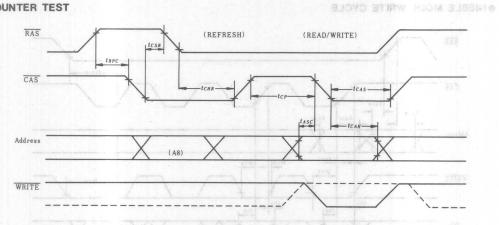
• HIDDEN REFRESH CYCLE



• CAS BEFORE RAS REFRESH CYCLE



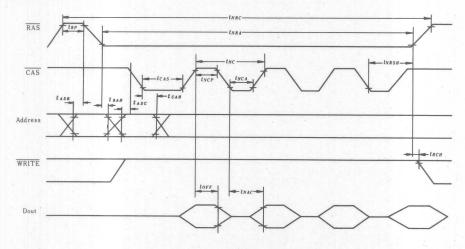
• COUNTER TEST



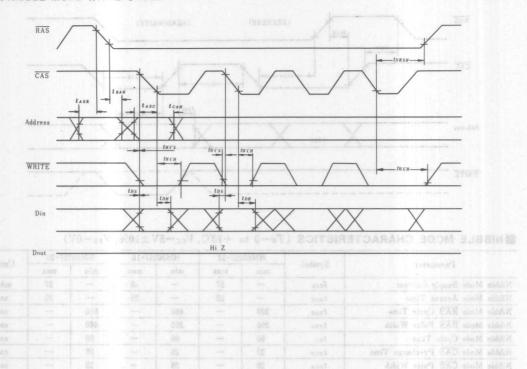
NIBBLE MODE CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm10\%$, $V_{ss}=0V$)

Parameter	Symbol HM502		257-12 HM50257-15		HM50257-20		Unit	
	Symbol	min	max	min	max	min	max	Unit
Nibble Mode Supply Current	Iccs	_	57		48	-	37	mA
Nibble Mode Access Time	tNAC		20		25	_	35	ns
Nibble Mode RAS Cycle Time	tNRC	390	_	460	_	590	_	ns
Nibble Mode RAS Pulse Width	tNRA	290	-	350	_	460	- 1	ns
Nibble Mode Cycle Time	tnc	50	-	60	_	80	_	ns
Nibble Mode CAS Precharge Time	tNCP	20	-	25	-	35	-	ns
Nibble Mode CAS Pulse Width	tnca	20	-	25	-	35		ns
Nibble Mode RAS Hold Time	tnrsh	40	-	45	_	55		ns

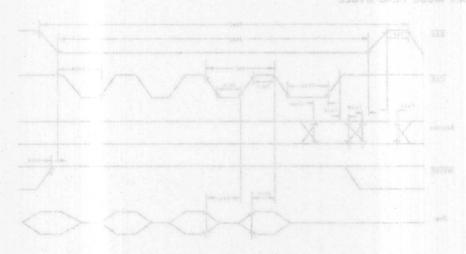
• NIBBLE MODE READ CYCLE



• NIBBLE MODE WRITE CYCLE



WIRELE MODE PEAD CYCLE



HNGISGAP, HNGISGAF

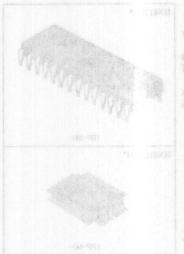
- o Single HIV Power Jumply

 The state Data Depart for OR-ries

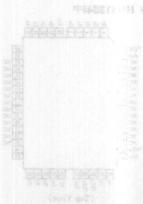


V			apa Voltage*
	-20 to +85	S Steep	

V			
- V			







HN61364P, HN61364FP

8192-word x 8-bit Mask Programmable Read Only Memory

The HN61364P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

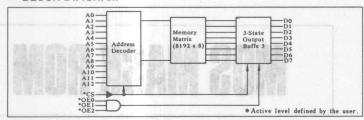
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS, $OE_0 \sim OE_2$ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

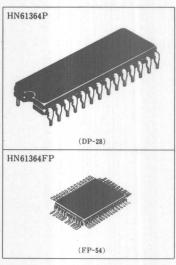
Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to +7.0	V
Input Voltage*	V_{in}	-0.3 to +7.0	V
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C
Bias Storage Temperature	Tbias	-20 to +85	°C

^{*} with respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

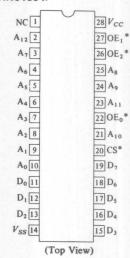
Item	Symbol	min	typ	max	Unit
Supply Voltage *	Vcc	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	-0.3	-	0.8	V
	V_{IH}	2.2	-	Vcc	V
Operating Temperature	Topr	-20	-	75	°C

^{*} with respect to Vss

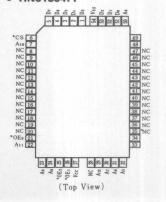


PIN ARRANGEMENT

HN61364P



HN61364FP



■ ELECTRICAL CHARAGTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_B = -20 to +75°C

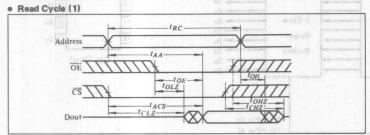
Item		Symbol	Test Condition	min	typ	max	Unit
Input High-level	Voltage	V_{IH}		2.2		Vcc	V
Input Low-level Voltage		VIL	cyramiable, byte-organized (acmor	-0.3	0.27.101	0.8	V
Output High-leve	l Voltage	V _{OH}	$I_{OH} = -205 \mu A$	2.4	SO CT LOS	JED FOLD	V
Output Low-level	l Voltage	VoL	I_{OL} =3.2mA	DIVE O	in Cakin	0.4	V
Input Leakage Current Output High-level Leakage Current		Iin	V_{in} =0 to 5.5V	11111	e sellio di BMATAN	2.5	μΑ
		I _{LOH}	V_{out} =2.4V, CS=0.8V, $\overline{\text{CS}}$ =2.2V	.31013			μA
Output Low-level	Leakage Current	ILOL	V_{out} =0.4V, CS=0.8V, $\overline{\text{CS}}$ =2.2V	SO ALD	ar. Jah	10	μA
Supply Current	Active	Icc *	V_{CC} =5.5V, I_{out} =0mA	da io	10	25	mA
Standby	I_{SB}	V_{CC} =5.5V, $\overline{\text{CS}} \ge V_{CC}$ -0.2V, CS \le 0.2V	WYOU II	1 2	30	μΑ	
Input Capacitanc	e	Cin	V_{in} =0V, f =1MHz, T_a =25°C	-	-	10	pF
Output Capacitance		Cout	in-0v, j-1MHz, 1 a=23 C			15	pF

^{*} steady state current

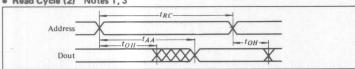
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE) $(V_{cc}=5V\pm10\%, V_{ss}=0V, T_a=-20 \text{ to } +75^{\circ}\text{C}, t_r=t_f=20\text{ns})$

Item	Symbol	min	max	Unit
Read Cycle Time	tRC	250	-	ns
Address Access Time	t _{AA}	-	250	ns
Chip Select Access Time	tACS	-	250	ns
Chip Selection to Output in Low Z	t _{CLZ}	10	noitered	ns
Output Enable to Output Valid	toE	-	100	ns
Output Enable to Output in Low Z	toLZ	10	-	ns
Chip Deselection to Output in High Z	t _{CHZ}	0	100	ns
Chip Disable to Output in High Z	toHZ	0	1.00	ns
Output Hold from Address Change	toH	10	-	ns

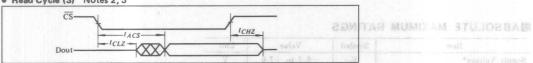
TIMING WAVEFORM



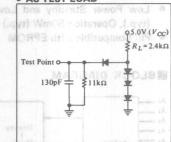




• Read Cycle (3) Notes 2, 3



AC TEST LOAD



Notes) 1. $t_r - t_f = 20 \text{ ns}$

- 2. C_L includes jig capacitance.
 - 3. All diodes are 1S2074®.

NOTES:

- 1. Device is continuously selected.
- 2. Address Vaild prior to or coincident with CS transition low.

 3. OE = V_{IL}

Operation Temperatus Storage Temperature

HN61365P

8192-word×8-bit Mask Programmable Read Only Memory

ELECTRICAL CHARASTERISTICS (V_{CC} = 5/±10%, V_{SS} = 6V, T_{a} = -20 to T_{c} °C

The HN61365P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS input and the memory content are defined by the user. The chip select input deselects the output and puts the chip in a power-down mode.

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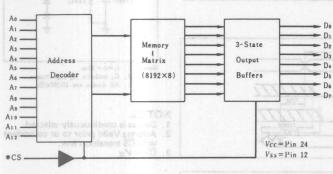
FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5 Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5µW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■PIN ARRANGEMENT



BLOCK DIAGRAM



* Active level defined by the user.

MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	
Supply Voltage*	Vcc	-0.3 to $+7.0$		
Input Voltage*	Via	-0.3 to +7.0	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tets	-55 to +125	°C	
Storage Temperature (under bias)	Thias	-20 to +85	°C	

* with respect to Vss

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	boof mindson	typ	max 8	Unit
Supply Voltage*	Vcc	4.5	5.0	5.5	V
Input Voltage*	VIL	-0.3	MATERIA BOND	0.8	V
	V_{IH}	2.2	SELECTION RATE (NO.)	Vcc	V
Operating Temperature	Topr	-20	ess serie rado	75	°C

^{*} With respect to Vss

ELECTRICAL CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $V_{ss}=0V$, $T_a=-20$ to $+75^{\circ}$ C) and only only of the second second

Item	Symbol	Test Conditions		min	typ	max	Unit
Input Voltage	V_{IH}			2.2		Vcc	V
	VIL			-0.3	-	0.8	V
Output Voltage	Von			2.4	noin w	Static Op	VIII V
Output voltage	Vol			- ys	DON'T LOV	0.4	v
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim 5.5 \text{V}$		BO 107 31	mut is	2.5	μΑ
Output Leakage Current	ILOH	CS=0.8V, CS =2.2V	Vout = 2.4V	eriil sutun	O stim	10	μA
Output Leakage Current	ILOL	CS=0.8V, $CS=2.2V$	$V_{out} = 0.4 \mathrm{V}$	-	- 14	10	μA
Active Supply Current	Icc*	$V_{cc}=5.5$ V, $I_{DOUT}=0$ mA		and the	10	25	mA
Stand by Supply Current	I_{SB}	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \text{ CS} \le 0$	$0.2V, V_{cc} = 5.5V$	A Mileston	1	30	μΑ
Input Capacitance	Cin	V -OV 6-1MIL T-	or°C	21/7/00	3 -4	10	pF
Output Capacitance	Cout	$V_{in} = 0 \text{ V}, \ f = 1 \text{ MHz}, \ Ta = 25^{\circ}\text{C}$		-	-	15	pF

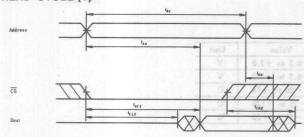
^{*} Steady state current

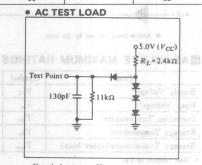
■ RECOMMENDED AC OPERATING CHARACTERISTICS

• READ SEQUENCE ($V_{cc} = 5V \pm 10\%$, $V_{ss} = 0V$, $T_a = -20$ to $+75^{\circ}$ C, $t_r = t_f = 20$ ns)

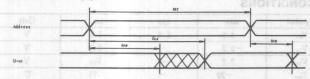
Item #	Symbol	min	max	Unit
Read Cycle Time	tRC	250	- 10	ns
Address Access Time	taa	_	250	ns
Chip Select Access Time	tacs		250	ns
Chip Selection to Output in Low Z	tcLZ	10		ns
Chip deselection to Output in High Z	tcHZ	0	100	ns
Output Hold from Address Change	t _{OH}	10		ns

• READ CYCLE (1)



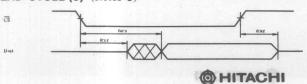


• READ CYCLE (2) (Notes 1)



Notes) 1. t_r−t_f−20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074⊕.

• READ CYCLE (3) (Notes 2)



Notes)

 Device is continuously selected
 Address Valid prior to or coincident with CS transition low.

HN61366P

8192-word×8-bit Mask Programmable Read Only Memory

The HN61366P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

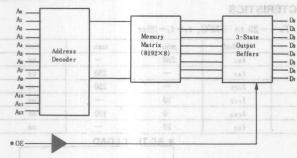
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the OE input and the memory content are defined by the user.

FEATURES

- Fully Static Operation
- Single +5V power supply
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Operation; 50mW (typ.)
- Pin Compatible with EPROM

BLOCK DIAGRAM



* Active level defined by the user.

MADSOLUTE MAXIMUM RATINGS

Value	Unit	Ī
-0.3 to +7.0	V	
-0.3 to +7.0	V	
-20 to +75	°C	
-55 to +125	°C	
-20 to +85	°C	
	-0.3 to +7.0 -20 to +75 -55 to +125	-0.3 to +7.0 V -20 to +75 °C -55 to +125 °C

* With respect to Vss

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	min typ		Unit
Supply Voltage*	Vcc	4.5	5.0	5.5	V
	VIL	-0.3		0.8	V
Input Voltage*	V_{IH}	2.2	XXX	Vcc	V
Operating Temprature	Topr	-20	==	75	°C

* With respect to Vss



PIN ARRANGEMENT



@READ CYCLE (2) (Notes 1)

@READ CYCLE (3) (Notes 2)

ELECTRICAL CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $V_{ss}=0V$, $T_a=-20$ to $+75^{\circ}$ C)

Item	Symbol	Test Condit	ions	min	typ	max	Unit
Only Memory	V_{IH}	Mass Programma	CONT. NO.	2.2	#0_10	Vcc	V
Input Voltage	Vil	no rid-8xiP9Eat or	-0.3	312518	0.8	V	
	V_{OH}	$I_{OH} = -205\mu\text{A}$	ago II Inome	2.4	mear St	PHT-CMC	V
Output Voltage	Vol	IoL=3.2mA	I _{OL} =3.2mA		is oo nng	0.4	V
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim 5.5 \text{V}$	H-suited for b	ew y n orr	am - ide	2.5	μΑ
0.44	ILOH	$OE=0.8V, \overline{OE}=2.2V$	$V_{OUT}=2.4V$	daretu	grace h	10	μΑ
Output Leakage Current	ILOL	OE=0.8V, $OE=2.2V$	$V_{our} = 0.4 \text{V}$	pel la ct in	gir la ov	10	μΑ
Operating Supply Current	Icc*	$V_{cc}=5.5$ V, $I_{out}=0$ mA	alo eneble inor	on bras	10	25	mA
Input Capacitance	Cin	$V_{in}=0$ V, $f=1$ MHz, $Ta=$	9F°C	Fina rid t	lio mois	10	pF
Output Capacitance	Cout	$V_{in}=0$ V, $j=1$ MHz, $Ia=$	25 0	-	_	15	pF

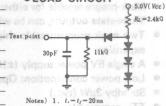
* Steady state current

■RECOMMENDED AC OPERATING CONDITIONS

• READ CYCLE ($V_{cc} = 5V \pm 10\%$, $V_{ss} = 0V$, $T_a = -20 \sim +75^{\circ}C$, $t_r = t_f = 20 \text{ ns}$)

Item	Symbol	min	max	Unit
Read Cycle Time	trc	250	la criercia i	ns
Address Access Time	taa		250	ns
Output Enable to Output Valid	toE		100	ns
Output Enable to Output in Low Z	toLZ	10	_	ns
Output Disable to Output in High Z	toHZ	. 0	100	ns
Output Hold from Address Change	t _{OH}	10	-	ns

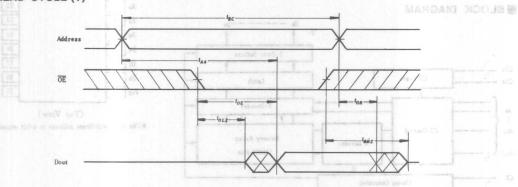




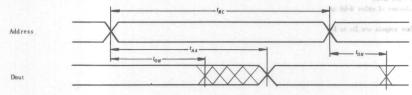
2. C_t includes jig capacitance.
3. All diodes are 1S2074 .

TIMING WAVEFORM

• READ CYCLE (1)



● READ CYCLE (2) Note 1)



Note) 1. $\overline{OE} = V_{IL}$

16384 × 8-bit or 32768 × 4-bit CMOS Mask Programmable Read Only Memory

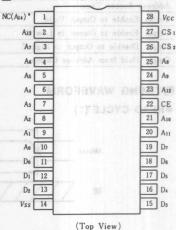
The Hitachi HN43128P is a mask programmable, 16384x8-bit or 32786x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL and DTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through two chip select inputs. Either active "High" or active "Low" of chip select inputs and a chip enable input is defined at mask level. The organization of 8 bit or 4 bit is designed by the user.



FEATURES

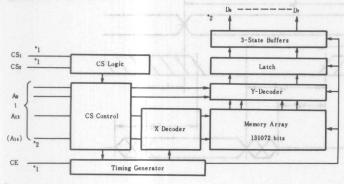
- Mask-programmable for either 4-bit or 8-bit organization.
- Three-state outputs, can be wired-OR.
- Two mask programmable chip select terminals facilitate memory expansion.
- A single 5V power supply (±10%).
- Low power consumption: Operation 3mW (typ.),
- Standby 3μW (typ.)
- TTL compatible
- Access time: 6.5μs (max)

PIN ARRANGEMENT



*The most significant address in 4-bit organization.

BLOCK DIAGRAM



^{*1} Active level defined at mask level.

In 4-bit organization, data outputs are Do to Da.

^{*2} Mask programmable selection of either 4-bit or 8-bit organization.

MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit Wash 110-8 X brow-
Supply Voltage*	Vcc	$-0.3 \sim +7.0$	ANSISISSOTT & AT STORES
Input Voltage*	Vin	$-0.3 \sim +7.0$	o per Aesto and ut est tot paulisep A
Operating Temperature Range	Topr	-20~+75	vice operat : (form a single power a
Storage Temperature	Tota	-55~+125	T. and require no clocks or 3- tree
Bias Storage Temperatore	Thias	-20~+85	The active (see of the Co. C. C.)

Note: * Referenced to Vss.

outgut said outs the thicken a power down made. **ELECTRICAL CHARACTERISTICS** ($V_{cc}=5V\pm10\%$, $V_{ss}=0V$, $T_a=-20\sim+75^{\circ}C$)

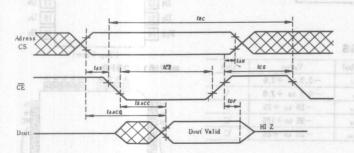
Item	Symbol	Test	Condition	min	typ	max	Unit
Input "High" Level Voltage	V_{IH}			2.4	00,000	Vcc	V
Input "Low" Level Voltage	VIL			0	nivoti isi	0.8	V.
Output "High" Level Voltage	V_{OH}	$I_{OH} = -100 \mu\text{A}$		2.4	owner Su	rio\ ⊏ 8+	V
Output "Low" Level Voltage	Vol	$I_{OL}=1.6\mathrm{mA}$	reiT	RO Tol 1	works U at	0.4	V
Input Leakage Current	Iin	$V_{in} = 0 \sim 5.5 \mathrm{V}$	Outrout Enable	tanin2 o	dO First	2.5	μA
Output "High" Level Leakage Current	I_{LOH}	CE = 0.8 V	$V_{out} = 2.4 \mathrm{V}$	-		5	μA
Output "Low" Level Leakage Current	ILOL	$\overline{\text{CE}} = 2.4\text{V}$	$V_{out} = 0.4 \mathrm{V}$	20/TAC	No. or all the	5	μA
In stand-by	I_{SB}	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V}$ $\text{CS} \ge V_{ss} + 0.2\text{V}$	$V_{cc} = 5.5 \text{V}$	off same file	1	30	μA
Supply Current In operation	Icc *	$t_{RC} = 7.5 \mu\text{s}$	$V_{cc} = 5.5 \text{ V}$	1.00/6/2	0.6	1.5	m A
Input Capacitance	Cin		II	Month Co	Tresta Lore	10	pF
Output Capacitance	Cout	$V_{in} = 0 \text{ V}, f = 1 \text{ M}$	Hz, Ta=25 C	E E Charle	19/20 Jan 19	12.5	pF

* Steady state current

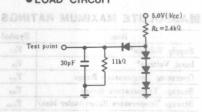
AC OPERATING CHARACTERISTICS

• READ SEQUENCE $(V_{CC} = 5V \pm 10\%, V_{SS} = 0V, T_a = -20 \text{ to } +75^{\circ}C, t_r = t_f = 20 \text{ ns})$

Item	Symbol	min	max	Unit
Read Cycle Time	t _{RC}	7.5	00000	μs
Address Access Time	tAACC	0	6.5	μs
Chip Enable Access Time	t_{EACC}		6.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μς
Address Set-up Time	tas	0.5	+	μs
Address Hold Time	t _{AH}	0	-	μs
Chip Enable ON Time	$t_{\overline{CE}}$	6.0	1 -	μs
Chip Enable OFF Time	d tce	1.0	1000000	μs



• LOAD CIRCUIT



Notes: 1. $t_r = t_f = 20 \text{ ns}$.

2. CL includes jig capacitance.

3. All diodes are 1S2074 (B).

HN613128P, HN613128FP

16384-word×8-bit Mask Programmable Read Only Memory

The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE0, OE1 input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

FEATURES

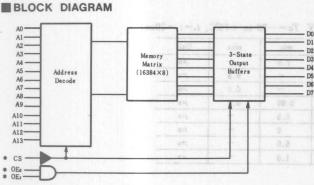
- **Fully Static Operation**
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation;

Standby:

5μW (typ.)

Operation: 50mW (typ.)

Pin Compatible with EPROM



* Active level defined by the user.

MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to $+7.0$	V
Input Voltage*	Vin	-0.3 to $+7.0$	V
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tets	-55 to +125	°C
Storage Temperature Range (under bias)	This	-20 to +85	°C

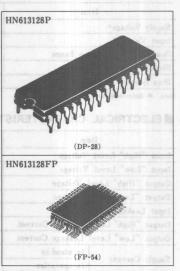
* With respect to Vss.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	Vcc	4.5	5.0	5.5	V
	VIL	-0.3	-	0.8	V
Input Voltage*	VIH	2.2	-	Vcc	V
Operating Temperature	Topr	-20	-	75	°C

* With respect to Vss.

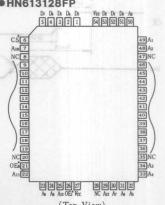
(1) HITACHI



PIN ARRANGEMENT



●HN613128FP



ELECTRICAL CHARACTERISTICS ($V_{cc}=5.0V\pm10\%$, $V_{ss}=0V$, $T_a=-20$ to $+75^{\circ}C$)

Item Item	Symbol	Test Condition	min	typ	max	Unit
Input High-level Voltage	VIH	on sid to work and a side of the and	2.2	per Fosta	Vcc	V
Input Low-level Voltage	VIL	- No Control and an analysis of the second	-0.3	-	0.8	V
Output High-level Voltage	Von	$I_{OH} = -205\mu\text{A}$	2.4	1	1100.00	V
Output Low-level Voltage	Vol	$I_{OL}=3.2\mathrm{mA}$	articum?	St. Tolico	0.4	V
Input Leakage Current	Iin	V _a = 0 to 5.5V	is illa	£-101111	2.5	μA
Output High-level Leakage Current	ILOH	$V_{out} = 2.4 \text{V}, \text{CS} = 0.8 \text{V}, \overline{\text{CS}} = 2.2 \text{V}$	GIOR <u>L</u> I	ALTERNATION OF THE PERSON OF T	10	μA
Output Low-level Leakage Current	ILOL	$V_{out} = 0.4 \text{V, CS} = 0.8 \text{V, } \overline{\text{CS}} = 2.2 \text{V}$	1010	uge 3	10	μΑ
Supply Current (Active/Standby)	Icc/ I.b	$V_{cc} = 5.5 \text{V}, I_{DOUT} = 0 \text{ mA} / \overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \text{CS} \le 0.2 \text{V}$	मारू क्या	10/1	25/30	mA/µA
Input Capacitance	Cin	$V_{in} = 0 \text{ V}, f = 1.0 \text{ MHz}, Ta = 25^{\circ}\text{C}$	RG 940	11/45 1	10	pF
Output Capacitance	Cout	$V_{in} = 0 \text{ V}, f = 1.0 \text{ MHz}, Ta = 25^{\circ}\text{C}$		-	15	pF

^{*} Steady state current

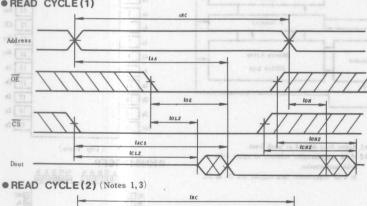
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

 $(V_{cc}=5.0V\pm10\%, V_{ss}=0V, T_{a}=-20 \text{ to } +75^{\circ}\text{C}, \text{All timing with } t_{r}=t_{f}=20 \text{ ns})$

	6 1 1	HN61	3128P	noisnao	
Item	Symbol	min	max	World Low as supply Vol.	
Read Cycle Time	trc	250	CANTHER TO DOS	ns more and a swood w	
Address Access Time	taa	_	250	ns (.qyr) Wild ydbno	
Chip Select Access Time	tacs	- 1	250	ns sidheqmoa "J	
Chip Selection to Output in Low Z	tcLZ	10	_	ns (XBIT) 21 C.C. comis acto	A B
Output Enable to Output Valid	toE	_	100	ns	
Output Enable to Output in Low Z	toLz	10		ns DARDAIG NOO	
Chip deselection to Output in High Z	tcHZ	0	100	ns	
Chip Disable to Output in High Z	toнz	0	100	ns	
Output Hold from Address Change	tон	10		ns	

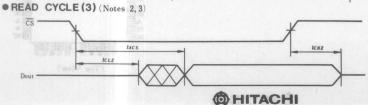
TIMING WAVEFORM

• READ CYCLE (1)

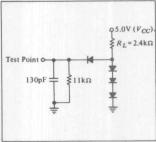


Dout

Address



AC TEST LOAD



- Notes) 1. $t_r = t_f = 20 \text{ ns}$.
 - C_L includes jig capacitance.
 All diodes are 1S2074[®].

NOTES:

ton

- 1. Device is continuously selected.
- 2. Address Valid prior to or coincident with CS transition low.
- 3. $\overline{OE} = VIL$.

HN61256P, HN61256FP

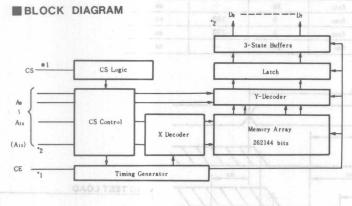
32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%)
- Low power consumption: Operation 7.5mW (typ.), Standby 5μ W (typ.)
- TTL compatible
- Access time: 3.5µs (max)

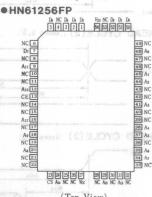
•HN61256P



- *1 Active level defined at mask level.
- *2 Mask programmable selection of either 4-bit or 8-bit organization.
 - In 4-bit organization, data outputs are Do to Da.



(Top View)



(Top View)

MASSITURE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	Vcc	-0.3~+7.0	V V
Input Voltage*	Vin	$-0.3 \sim +7.0$	V has
Operating Temperature Range	Topr	0~+75	°C
Storage Temperature Range	Tsis	-55~+125	°C
Bias Storage Temperature Range	Thias	-20~+85	°C

Note: * Referenced to V_{ss} .

■ ELECTRICAL CHARACTERISTICS

 $(V_{cc}=5V\pm10\%, V_{ss}=0V, T_a=0\sim+75^{\circ}C)$

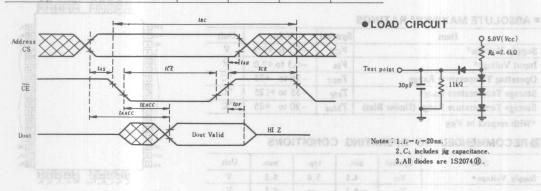
It	em	Symbol	Test C	Condition	min	typ	max	Unit
Input "High" Level	Voltage	V_{IH}			2.4		Vcc	V
Input "Low" Level	Voltage	V_{IL}			0		0.8	V
Output "High" Leve	l Voltage	V_{OH}	$I_{OH} = -100 \mu\text{A}$		2.4	udaha <u>n</u>		V
Output "Low" Leve	l Voltage	Vol	$I_{OL}=1.6\mathrm{mA}$		CIO IOI	advar.	0.4	V
Input Leakage Curr	ent	Iin	$V_{in} = 0 \sim 5.5 \text{ V}$	CI TRICHIO DUI	300 <u>10</u> 0 U	BELLE FLUE	2.5	μΑ
Output "High" Leve	l Leakage Current	I_{LOH}	CE = 0.8 V	$V_{out} = 2.4 \mathrm{V}$	-	- 9	5	μΑ
Output "Low" Leve	l Leakage Current	ILOL	$\overline{\text{CE}} = 2.4 \text{V}$	$V_{out} = 0.4 \mathrm{V}$	SIMGZ	SBALLET #5	5	μA
c 1 c . 7W	In stand-by	I_{SB}	$\overline{CS} \ge V_{cc} - 0.2 \text{ V.}$ $\overline{CS} \ge V_{ss} + 0.2 \text{ V.}$	Power Operat	MOT DO	s von	30	μΑ
Supply Current	pply Current In operation I_{CC}^* $t_{RC} = 4.0 \mu\text{s}$ $V_{CC} = 5.5$	Vcc=5.5V	d nows	1.5	3.0	m A		
Input Capacitance		Cin	W -0W (-1MU	I - T - 95°C	WOR	SE PEN	10	pF
Output Capacitance	D.	Cout	$V_{in} = 0 \text{ V}, f = 1 \text{ MHz}, Ta = 25 ^{\circ}\text{C}$		-	-	12.5	pF

tooserdon, to

AC OPERATING CONDITION AND CHARACTERISTICS

• READ SEQUENCE $(V_{cc}=5V\pm10\%,\ V_{ss}=0V,\ T_a=0\sim+75^{\circ}C,\ t_r=t_f=20\,\text{ns})$

Item	Symbol	min	max	Unit
Read Cycle Time	t RC	4.0		μs
Address Access Time	tAACC	-	3.5	μs
Chip Enable Access Time	t eacc	- 1	3.0	μs
Data Hold Time from Address	t DF	0.05	0.5	μs
Address Set-up Time	tas	0.5	-	μs
Address Hold Time	t _{AH}	0	_	μs
Chip Enable ON Time	t CE	3.0	Rob lo r ol ov	μs
Chip Enable OFF Time	t CE	0.5	-	μs



^{*} Steady state current

HN613256P, HN613256FP

32768-word x 8-bit Mask Programmable Read Only Memory

The HN613256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized system.

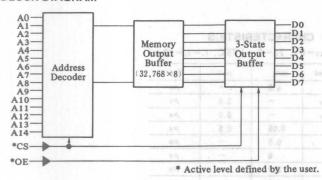
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks nor refreshing because of static operation.

The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 250ns
- Low Power Standby and Low Power Operation;
 Standby 5µW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



(FP-54)

PIN ARRANGEMENT



* Active level can be defined by the customer.

• HN613256FP

ABSOLUTE MAXIMUM RATINGS

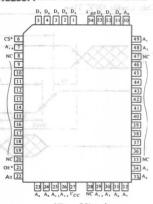
(Sal)Wo.8 O . Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to +7.0	V
Input Voltage*	Vin	-0.3 to +7.0	V
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-55 to +125	°C
Storage Temperature Range (Under Bias)	Thias	-20 to +85	°C

^{*}With respect to Vss

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	Vcc	4.5	5.0	5.5	V
7 . 17 1	VIL	-0.3	_	0.8	V
Input Voltage*	VIH	2.2	-	Vcc	V
Operating Temperature	Topr	-20		75	°C

^{*} With respect to Vss.



(Top View)

* Active level can be defined by the customer.

e TTL Companists

Maximum Access Time-350ns

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{V} \pm 10\%$, $V_{SS} = 0 \text{V}$, $T_a = -20 \sim +75 \,^{\circ}\text{C}$)

It	em	Symbol	Test C	ondition	min	typ	max	Unit
Y 37 - 14	HER RETURNS	V _{IH}	To facilitate use th	bus-organized systems	2.2	0.70	VCC	V
Input Voltage		V_{IL}	rise compositibility visi	s single names supply lyac nominality utility utility		OTE:	0.8	V
Output Voltage		VOH	$I_{OH} = -205 \mu A$	chineles or refreshing	2.4	8701	bas	V
Output voltage		VOL	I _{OL} = 3.2 mA	non vocasam edt bon e	rta71S	Chic	0.4	V
Input Leakage C	urrent	Iin	$V_{in} = 0 \sim 5.5 \text{V}$	o input desclares the or	de n a	nano	2.5	μА
Output Leakage	Current	ILOH	$CS = 0.8V$, $\overline{CS} = 2.2V$	V _{out} = 2.4V	10175.00	V/ND-	10	μA
Output Leakage	Current	ILOL	CS - 0.6V, CS - 2.2V	$V_{out} = 0.4V$	-	-	10	μA
Supply Current	Active	Icc*	$V_{CC} = 5.5 \text{V}, I_{out} = 0 \text{ m}$	A	-	10	30	mA
Supply Current	Standby	I _{SB}	$V_{CC} = 5.5 \text{V}, \overline{\text{CS}} \ge V_{CC}$	$c - 0.2$ V, CS ≤ 0.2 V	n Tales	1	30	μΑ
Input Capacitan	ce	Cin	V - OV f- 1 MU T	- 25°C #W0C	permos	offic	10	pF
Output Capacita	nce	Cout	$V_{in} = 0V, f = 1 \text{ MHz}, T_a = 25 ^{\circ}\text{C}$		e stale	V-284	15	pF

^{*} Steady state current

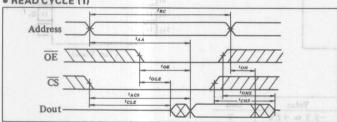
Preliminary

■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

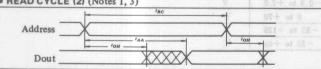
 $(V_{cc}=5V\pm10\%, V_{ss}=0V, T_a=-20\sim+75^{\circ}C, t_r=t_f=20ns)$

Item	Symbol	min	max	Unit					Lower
Read Cycle Time	tRC	250	-	ns	a. Zbn il				ansis
Address Access Time	tAA	-	250	ns					
Chip Select Access Time	tACS	-	250	ns		OCK DIAGRAM			
Chip Selection to Output in Low Z	tCLZ	10	-	ns					
Output Enable to Output Valid	toE	-	100	ns	LE				
Output Enable to Output in Low Z	tolz	10	-	ns					
Chip Deselection to Output in High Z	tCHZ	0	100	ns					Land A
Chip Disable to Output in High Z	toHZ	0	100	ns	eldecol.	shright (9:xx)			1 A
Output Hold from Address Change	tOH	10	-	ns					

TIMING WAVEFORM READ CYCLE (1)



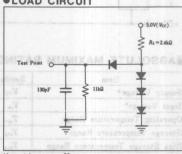
• READ CYCLE (2) (Notes 1, 3)



• READ CYCLE (3) (Notes 2, 3)



LOAD CIRCUIT



Notes: 1. $t_1 - t_1 - 20 \text{ ns}$

- 2. CL includes jig capacitance
- 3. All diodes are 1S2074®

NOTES:

- 1. Device is continuously selected.
- Address Valid prior to or coincident with CS transition low.
- 3. $\overline{OE} = VIL$.

HN62301P

131,072-word×8-bit Mask Programmable Read Only Memory

The HN62301P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The Chip Enable and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

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FEATURES

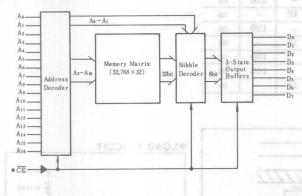
- Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time-350ns
- Lower Power Standby and Low Power Operation;
 Standby: 2mW (typ.), Operation: 75mW (typ.)

ower Power Standby and Low Power Operation:



(30930038 GA3A) 20011 GAGO 2 PIN ARRANGEMENT MOCER 4

BLOCK DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to $+7.0$	V
Input Voltage*	Vin	-0.3 to $+7.0$	V
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tats	-55 to +125	°C
Bias Storage Temperature Range	Thias	-20 to +85	°C

^{*} With respect to Vss

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales

Please contact your nearest Hitachis Sales Dept, regarding specifications.



■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70° C)

Item	Symbol	min	typ	max	Unit
Supply Voltage *	Vcc	4.5	5.0	5.5	V
	VIL	-0.3	V/-	0.8	V
Input Voltage*	V _{IH}	2.2		Vcc	V

^{*} with respect Vss

ELECTRICAL CHARACTERISTICS $(V_{cc}=5V\pm10\%, V_{ss}=0V, Ta=0 \text{ to } +70^{\circ}\text{C})$

Item	Symbol	Tes	t Conditions	min	typ	max	Unit
Normal Operating Current	Icci*	$t_{RC1} = \min$, $V_{CC} = 5.5$ V, $I_{out} = 0$ mA		-	15	50**	mA
Nibble Operating Current	Iccz*	$t_{RC2} = \min, \ V_{CC} = 5.5 \text{V}, \ I_{out} = 0 \text{mA}$		-	15	50**	mA
Stand by Current	I_{SB}	$\overline{\text{CE}} \ge V_{cc} - 0.2 \text{V}$, $V_{cc}=5.5V$	1-1	0.4	10	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V,	other OV	-10		10	μΑ
0	I_{LOH}	CE 0.0V	Vout = 2.4V	-	_	10	μΑ
Output Leakage Current	ILOL	CE=2.2V	$\overline{\text{CE}} = 2.2\text{V}$ $V_{\text{out}} = 0.4\text{V}$		-	10	μΑ
0	Von	$I_{out} = -205\mu A$		2.4			V
Output Voltage	Vol	Iout = 3.2mA		X	-	0.4	V

^{*} Steady state current

ECAPACITANCE $(V_{cc}=5V\pm10\%, T_a=25^{\circ}C, 1MHz, V_{in}=0V)$

Item	Symbol	typ	max	Unit
Input Capacitance (A ₀ ~A ₁₆ , \overline{CE})	Cin	TBD	10	лочо рЕдение
Output Capacitance (Do~D7)	Cout	TBD	15	pF

AC CHARACTERISTICS $(V_{cc}=5V\pm10\%, V_{ss}=0V, T_a=0 \text{ to } +70^{\circ}\text{C}, t_r=t_f=20\text{ns})$

Mode	Item	Symbol	min	max	Unit
****	Cycle Time	tRCI	350		ns
Normal	Address Access Time	tAA1		350	ns
	Data Hold Time	toн	10		ns
	CE Access Time	tACE		350	ns
	CE Enable Pulse Width	///tcE//X	350	Post	ns
CE	CE Disable Pulse Width	t _{CE}	15**	-	ns
CE operation	Address Set up Time	tas	0		ns
	Data Hold Time from CE	tcHZ	10**	GAGS TEET	0A ns
	Data Set Time from CE	tcLZ	10	-	ns
Nikkla	Nibble Address Access Time*	t _{AA2}	(201) 10 20	50	ns
Nibble operation	Nibble Cycle Time	t _{RC2}	50		ns
Turn-on & Turn-of	f Time	t _T		40	ns

^{*} Nibble Address Ao, A1



ones) 1. t.-ty-20ms 2. Cr meludus lis suppellant 3. All diedes are 1872/443.

^{* *} TBD

^{**} TBD

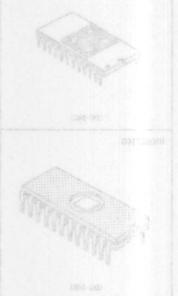
TIMMING CHART ●NORMAL CYCLE (CE=Low) Address -taal-Valid Data Previous Data OCE CYCLE CE Output Voltage Address HI CAPACITAZ IR Dout Valid Data ONIBBLE CYCLE A2~A16 Ao, Aı tAA2-Valid Data Previous Data Dout AC TEST LOAD 95.0V (VCC) $R_L = 2.4k\Omega$ Test Point 0-130pF ≠ \$11kΩ Notes) 1. $t_r = t_f = 20 \text{ ns}$ C_L includes jig capacitance. All diodes are 1S2074[®].

HN462716, HN4627166

2048-word × 8-bit U.V. Brasobie and Electrically Programmable 5 ead.

The HR682716 is a 2046 word by 8 bit erasoble and electrically programmable RCMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the only to ultraviolet light to erase the bit pattern.

- Single Power Supply ... +5V ±5%
- 2 Simple Programming ---- Program Voltage: +26V DC
 - * Static No Clocks Required
- Inputs and Outputs TTL Compatible Diging Both Read and Pregram Wode:
 - Fully Decoded on Chip Address Decode
 - Access Time 450ns Max.
 - Low Povior Dissipation -- SSSmW Max, Active Power
 191-mW Max Active Power
 - # Three State Output OR- Tie Capability
 - Interchangeable with Intel 2716



MOS PROM

10110	121		2 12
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	131		
ALLIA NOSIS TREEST		X Descries	
			1-01

MPROGRAMMING OPERATION

		Vap (21)		Outputs (9-11.13-17)
Descleet				
		4-5		High Z
	Policed Visite Fig.	+25		
Program Ve			2+	

MARSOLUTE MAXIMUM RATINGS

		Operating Temperature Range
		Storage Temperature Name
	V+ 01 E.D -	All Input and Output Voltages"
ST.	-0.3 to +78	Voy Samply Voltage*

^{*} Will respect to Ground





HN462716, HN462716G

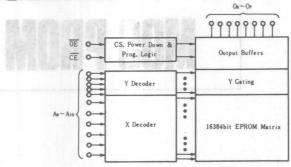
2048-word × 8-bit U.V. Erasable and Electrically Programmable Read Only Memory

The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent-lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

- Single Power Supply · · · · +5V ±5%
- Simple Programming · · · · Program Voltage: +25V DC
 Programs with One 50ms Pulse
- Static · · · · · · No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time · · · · · · 450ns Max.
- Low Power Dissipation 555mW Max. Active Power 161mW Max. Standby Power
- Three State Output · · · · · OR- Tie Capability
- Interchangeable with Intel 2716

(DC-24C) HN462716G (DC-24C) (DG-24B)

BLOCK DIAGRAM



■ PROGRAMMING OPERATION

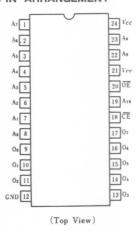
Pins	(18)	OE (20)	V _{PP} (21)	Vcc (24)	Outputs (9~11, 13~17)
Read	VIL	VIL	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	VIH	Don't Care	+5	+5	High Z
Program	Pulsed VIL to VIH	V_{IH}	+25	+5	Din
Program Verify	VIL	VIL	+25	+5	Dout
Program Inhibit	VIL	V_{IH}	+25	+5	High Z

MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	
Operating Temperature Range	g Temperature Range Top,		°C	
Storage Temperature Range	Tate	-65 to +125	°C	
All Input and Output Voltages*	V _T	-0.3 to +7	V	
VPP Supply Voltage*	V_{PP}	-0.3 to $+28$	V	

* With respect to Ground

PIN ARRANGEMENT



OTYPICAL CHARACTERSTICS

READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm5\%$, $V_{PP}=V_{cc}\pm0.6V$)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	$V_{IN} = 5.25 \text{ V}$			10	μ·A
Output Leakage Current	ILO	Vour=5.25 V/0.4 V			10	μΑ
VPP Current	IPP1	$V_{PP} = 5.85 \mathrm{V}$	-	-	5	m A
Vcc Current (Standby)	Icci	$\overline{\text{CE}} = V_{IH}, \overline{\text{OE}} = V_{IL}$	-	13	25	m A
Vcc Current (Active)	Iccz	$\overline{OE} = \overline{CE} = V_{IL}$		56	100	m A
Input Low Voltage	VIL		-0.1		0.8	V
Input High Voltage	VIH		2.0	-	Vcc+1	V
Output Low Voltage	Vol	$I_{OL}=2.1\mathrm{mA}$		-	0.4	V
Output High Voltage	Vон	$I_{OH} = -400 \mu\text{A}$	2.4	- L		V

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

• AC CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm5\%$, $V_{PP}=V_{cc}\pm0.6V$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address to Output Delay	tacc	$\overline{OE} = \overline{CE} = V_{IL}$		1 + 1	450	ns
CE to Output Delay	t CE	$\overline{OE} = V_{IL}$	-	11+1	450	ns
OE to Output Delay	toe	$\overline{\text{CE}} = V_{IL}$			120	ns
OE High to Output Float*	tor	$\overline{\text{CE}} = V_{IL}$	0	mb-state and	100	ns
Address to Output Hold	toн	$\overline{OE} = \overline{CE} = V_{IL}$	0	1 + 1	1 1	ns

^{*:} t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• CAPACITANCE ($Ta=25^{\circ}C, f=1MHz$)

Item (NY) 5259	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	Cin	$V_{IN} = 0 \text{ V}$	-	6	pF
Output Capacitance	Cout To	Vour=0V	naga u n.	12	pF

SWITCHING CHARACTERISTICS

Test Conditions

Am Input Pulse Levels:

Input Rise and Fall Times:

Output Load:

Output Load:

Reference Level for Measuring Timing:

≤ 20 ns

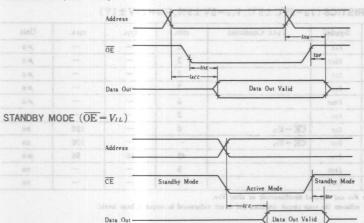
1TTL Gate + 100 pF

0.8V to 2.2V

Inputs 1V and 2V

Outputs 0.8V and 2V

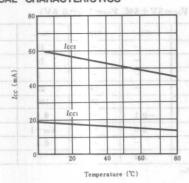
READ MODE $(\overline{CE} = V_{IL})$

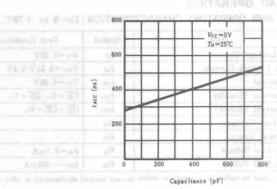


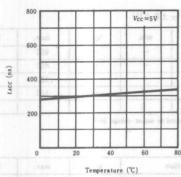
Input Leakage Carront

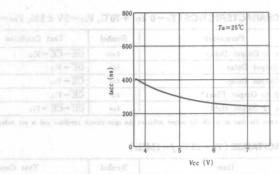
Program Pulse Rise Time

• TYPICAL CHARACTERISTICS









• DC PROGRAMMING CHARACTERISTICS ($Ta=25^{\circ}C\pm5^{\circ}C$, $Vcc=5V\pm5\%$, $Vpp=25V\pm1V$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	$V_{IN} = 5.25 \mathrm{V}$	_	_	10	μA
VPP Supply Current	I_{PP1}	$\overline{CE} = V_{IL}$ VS.S at V8.0	_	— tale	wad as 5 9	igni mA
VPP Supply Current During Programming	I _{PP2}	$\overline{\text{CE}} = V_{IH}$	_	ascell Title	30	m A
Vcc Supply Current	Icc	TITL Gate + 100 pt	-	_	100	m A
Input Low Level	VIL	VS bits VI Studini	-0.1	(11/28/2 <u>18</u> (1-2-1)	0.8	V
Input High Level	VIH	A7 DES ATO SIDATIO	2.0	_	$V_{cc}+1$	V
THE PROPERTY OF THE PARTY OF TH					I CE - VI	SAD MODE

• AC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C}\pm5^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm5^{\circ}$, $V_{PP}=25\text{V}\pm1\text{V}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	tas		2	- 10	_	μs
OE Setup Time	toes	-	2	_	_	μs
Data Setup Time	tos		2	_	_	μs
Address Hold Time	- t лн	fetay sid and	2	tomorphy() prof	_	μs
OE Hold Time	t oeh		5	_	_	μs
Data Hold Time	t DH		2	T.W	- 30) Hadi	μs ATS
OE to Output Float Delay*	tor	$\overline{\text{CE}} = V_{IL}$	0	-	120	ns
OE to Output Delay	toE	$\overline{\text{CE}} = V_{IL}$		_	120	ns
Program Pulse Width	t pw -		45	50	55	ms
Program Pulse Rise Time	t PRT		5	_	-	ns
Program Pulse Fall Time	tPFT	V	santi 5 three c	- 3	_	ns

Notes: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

^{*:} tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

a new pattern can then be written into the device.

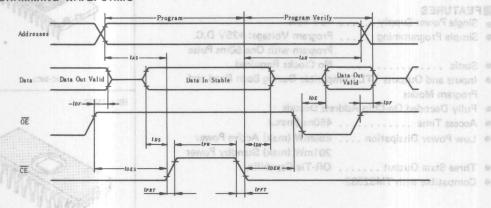
SWITCHING CHARACTERISTICS

Test Conditions

The HN462532 is a 4036 word by 8 bit erasable and electrically Input Pulse Level: 0.8V to 2.2V Input Rise and Fall Times:

≤ 20 ns 6011-31-16Ub (nig-AS & all begaloss) a solveb and (MOR siderums apong Output Load: 1 TTL Gate + 100 pF to a self-secula bil the recent self. bil the recent of the seculation Reference Level for Measuring Timing: American arranged the safe of right relative the of clina and records Inputs; 1V and 2V, Outputs; 0.8V and 2V

PROGRAMMING WAVEFORMS



OFRASE

Erasure of HN462716 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm2

DEVICE OPERATION

READ MODE

Dataout is available 450ns (t'ACC) from addresses with OE low or 120ns (toE) from OE with addresses stable.

DESELECT MODE

The outputs may be OR-tied together with the other HN462716s. When HN462716s are deselected, the OE inputs must be at high TTL level.

POWER DOWN MODE

Power down is achieved with CE high TTL level, In this mode the outputs are in a high impedance state.

PROGRAMMING

Initially, and after each erasure, all bits of the HN462716 are in the "High" state (Output High). Data is introduced by selectively programming "low" into the desired bit locations. In the programming mode, Vpp power supply is at 25V and OE input is at high TTL level. Data to be programmed are presented 8-bits in parallel, to the data output lines (00 to 07).

The addresses and inputs are at TTL levels.

After the address and data setup, a 50 ms, active high program pulse is applied to the CE input. The CE is at TTL level.

The HN462716 must not be programmed with a DC signal applied to the CE input.

PROGRAM VERIFY

The HN462716 has a program verify mode. A verify should be performed on the programmed bits to determine that they were correctly programmed. In this mode Vpp is at 25V.

PROGRAM INHIBIT

Programming of multiple HN462716s in parallel with different data is easily accomplished by using this mode. Except for CE, all like inputs of the parallel HN462716s may be common.

A TTL program pulse applied to a HN462716's CE input will program that HN462716. A low level CE inhibits the other HN462716s from being programmed.

HN462532, HN462532G

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN462532 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

FEATURES

Single Power Supply +5V ±5%

Simple Programming Program Voltage: +25V D.C.

Program with One 50ms Pulse

Static No Clocks Required

 Inputs and Outputs TTL Compatible During Both Read and **Program Modes**

Fully Decoded On-Chip Address Decode

Access Time 450ns (max.)

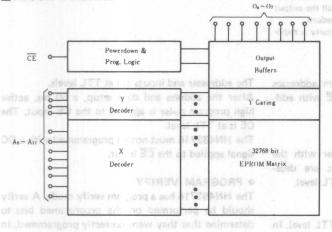
Low Power Dissipation 858mW (max) Active Power

201mW (max) Standby Power

Three Stste Output OR-Tie Capability

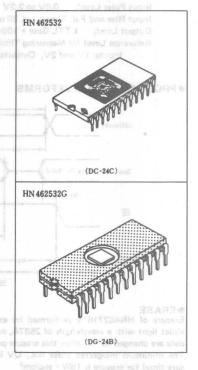
Compatible with TMS2532

BLOCK DIAGRAM



MODE SELECTION

Pins	(20)	V _{PP} (21)	Vcc (24)	Outputs (9 to 11, 13 to 17)	(Top View) 100 144
Read	VIL.	+5	+5	Dout	tive62716 are in the "High" state
Stand by	SEE SEE VIH TOTAL	+5	+5	High 7	Data is introduced by salactively
Program	Pulsed VIH to VIL	+25	+5	Din	"low" into the deaned bit lonetions."
Program Inhibit	VIH	+25	+5	High Z	ning mode. Vop nawer supply la



PIN ARRANGEMENT

	POOM DA
A7 1	picisliava 24 Ver
A6 2	23 As
As 3	22 A9
A4 4	21 Vr
A3 5	GOM TO 20 CE
A2 6	4 VSFD 23 19 A10
Ai 7	AI 4627165
Ao 8	augni 30 17 07
()0 9	16 ()6
O ₁ 10	15 Os
02 11	14 04
GND 12	13 ()3

■ ABSOLUTE MAXIMUM RATINGS

(VItem Comment of the control of the	Symbol	Value	Unit
All Input and Output Voltages*	no las V _T	-0.3 to +7	V Parestel
V _{PP} Voltage*	V_{PP}	-0.3 to +28	V.
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tate	-65 to +125	°C
With respect to GND.			Live Town 7

READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5$ V $\pm 5\%$, $V_{PP}=V_{cc}\pm 0.6$ V)

Parameter	Symbol	Test Condition	MIT COST	min	typ	max	Unit
Input Leakage Current	Iu	$V_{in} = 5.25 \mathrm{V}$	lodens	-	- 1	10	μΑ
Output Leakage Current	ILO	$V_{out} = 5.25 \text{V} / 0.4 \text{V}$	20	-	_	10	μΑ
VPP Current	I_{PP1}	$V_{PP} = 5.85 \mathrm{V}$	100	-	-	12	m A
Vcc Current (Standby)	Icci	$\overline{\text{CE}} = V_{IH}$		-	_	25	m A
Vcc Current (Active)	Icc 2	$\overline{\text{CE}} = V_{IL}$	100	-	-	150	m A
Input Low Voltage	V _{IL}		1/9/11	-0.1	_	0.8	Set V The
Input High Voltage	V _{IH}		9395	2.0	-0.00	$V_{cc}+1$	V
Output Low Voltage	V _{OL}	$I_{OL}=2.1\mathrm{mA}$	1879	-	-	0.4	la V
Output High Voltage	V _{OH}	$I_{OH} = -400 \mu\text{A}$. 191	2.4	-	projekt water	V

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

• AC CHARACTERISTICS (Ta=0 to ± 70 °C, $V_{cc}=5$ V ± 5 %, $V_{PP}=V_{cc}\pm 0.6$ V)

Parameter	Symbol	Test Condition	min	typ	max	Uhit
Address to Output Delay	tacc	$\overline{\text{CE}} = V_{IL}$	ROTTON	BTOARA	450	ns
CE to Output Delay	tce		-	-	450	ns
CE High to Output Float*	tor	VS.5 of V8.0	0	_	100	ns
Address to Output Hold	toн	$\overline{\text{CE}} = V_{IL}$	0	MANAGE THE	1 bos esiF	ns

*: Low defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Levels:

Input Rise and Fall Times:

Output Load:

Reference Level for Measuring Timing:

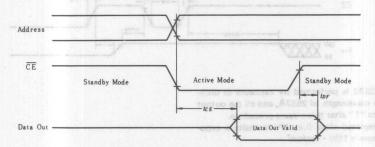
0.8V to 2.2V

≤ 20 ns

1TTL Gate + 100pF

Inputs; 1V and 2V,

Outputs; 0.8V and 2V



• CAPACITANCE ($Ta=25^{\circ}\text{C}, f=1\text{MHz}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	·Vin = 0 V	-	-	6	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}$	-	-	12	pF

PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS $(T_a=25^{\circ}\text{C}\pm5^{\circ}\text{C}, V_{cc}=5\text{V}\pm5\%, V_{PP}=25\text{V}\pm1\text{V})$

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	$V_{in} = 5.25 \text{V} / 0.4 \text{V}$	_		10	μΑ
VPP Supply Current During Programming	I _{PP2}	$\overline{\text{CE}} = V_{IL}$	_	98001 5	30	mA
Vcc Supply Current	Icc	pol pol		WEEK!	150	mA
Input Low Level	V_{IL}		-0.1	_	0.8	V
Input High Level-	V_{IH}		2.0	MOIT	Vcc+1	V

E ABSOLUTE MAXIMUM RATINGS

• AC PROGRAMMING CHARACTERISTICS ($T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, $V_{cc} = 5\text{V} \pm 5\%$, $V_{PP} = 25\text{V} \pm 1\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	tas	Var = 5, 25 V / 0, 4 V	2	- 10190	alog e C an	μs
Data Setup Time	tos	V28.3=49V 1 re	2	-		μs
Address Hold Time	t _{AH}	co r CE - Via	2	- 1	(Spand) to	μs
Data Hold Time	t _{DH}	$c_0 = \overline{GE} = V_{LL}$	2	_	evilo d) la	μs
Setup Time from VPP	tvpps		0	_	Voltage	ns
Program Pulse Hold Time	t PRH		0	_	sgaffeV	ns
VPP Hold Time	tvppн	Am1.3- ot	0	-	w Voltage	ns
Program Pulse Width	t pw	£ × 001 u.1	45	50	55	ms
Program Pulse Time	tPRT	and restored simultaneously or offer V.	5	s-constitutes	fellings ad re	ns
Program Pulse Time	tpfT		5	_	_	ns

• SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level:

Input Rise and Fall Times:

Output Load:

Reference Level for Measuring Timing:

0.8V to 2.2V

≤ 20 ns

1TTL Gate + 100pF Inputs; 1V and 2V,

Outputs; 0.8V and 2V

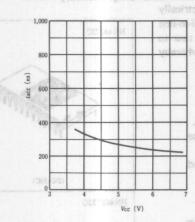
· SWITCHING CHARACTERISTICS Address Data Out Data In Data Out CE tvpps

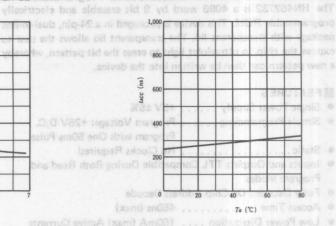
Erasure of HN462532 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm2.

					CAPACITIANCE (Targetto)
Xistor		Test Condition			To Francisco
			V.0,V	3	Impot (Lappoilance



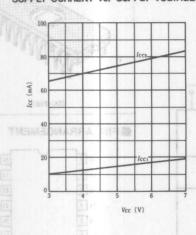
ACCESS TIME vs. SUPPLY VOLTAGE

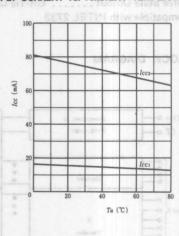




SUPPLY CURRENT vs. SUPPLY VOLTAGE

nA (max) Standby Cur SUPPLY CURRENT VS. AMBIENT TEMPERATURE





HN462732, HN462732G

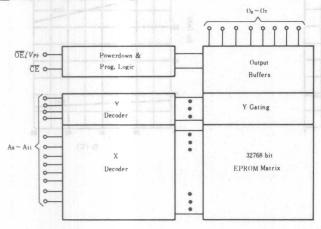
4096-word × 8-bit U.V. Erasable and Programmable Read Only Memory

The HN462732 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

FEATURES

- Single Power Supply +5V ±5%
- Simple Programming Program Voltage: +25V D.C.
 Program with One 50ms Pulse
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time 450ns (max)
- Low Power Dissipation 150mA (max) Active Currents
 30mA (max) Standby Current
- Three State Output OR-Tie-Capability
- Compatible with INTEL 2732

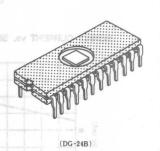
BLOCK DIAGRAM



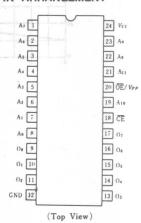
MODE SELECTION

Pins	(18)	OE /V _{PP} (20)	Vcc (24)	Outputs (9~11, 13~17)
Mode	(10)	(20)	(24)	(9-11, 13-17)
Read	VIL	VIL	+5	Dout
Stand by	VIH	Don't Care	+5	High Z
Program	VIL	V _{PP}	+5	Din
Program Verify	VIL	VIL	+5	Dout
Program Inhibit	VIH	V_{PP}	+5	High Z





PIN ARRANGEMENT



MPROGRAMMING OPERATION

■ ABSOLUTE MAXIMUM RATINGS

Item		Sym	Symbol Value		Unit	
Operating Temperature Range	mainhea	Topr	Symbol	0 to +70	°C	
Storage Temperature Range	74.0	Tata	- do	-65 to +125	Leal D'e Current	Frant
All Input and Output Voltage*	STUL S	$A = V_T$	View	-0.3 to $+7$	and squileV Ves.	Ostranio
VPP Voltage*	A.	OE /V	PP A	-0.3 to +28	red made V V	mq2m0

* With respect to GND

READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5$ V $\pm 5\%$, $V_{PP}=V_{cc}\pm 0.6$ V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current (Except $\overline{\text{OE}}/V_{PP}$)	I_{LI1}	$V_{IN} = 5.25 \mathrm{V}$	amaga	NO THE	10	μA
OE/VPP Input Leakage Current	ILI2	$V_{IN} = 5.25 \mathrm{V}$		-	10	μA
Output Leakage Current	ILO	$V_{out} = 5.25 \text{ V}$	-	152-25	10	μA
Vcc Current (Standby)	Iccı	$\overline{\text{CE}} = V_{IH}, \overline{\text{OE}} = V_{IL}$	-	-	30	mA
Vcc Current (Active)	Iccz	$\overline{OE} = \overline{CE} = V_{IL}$	-	-	150	mA
Input Low Voltage	VIL	mit i	-0.1	-	0.8	V
Input High Voltage	VIH	341	2.0	-	$V_{cc}+1$	V
Output Low Voltage	Vol	$I_{OL}=2.1\mathrm{mA}$	-	-1	0.45	V
Output High Voltage	V _{OH}	$I_{OH} = -400 \mu\text{A}$	2.4	-	om/T	Hold V

• AC CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5$ V $\pm 5\%$, $V_{PP}=V_{cc}\pm 0.6$ V)

em 88 Parameter 88	Symbol	Test Condition	min	typ	max	Unit
Address to Output Delay	tACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	nimakagor	1 political	450	ns
CE to Output Delay	tcE	$\overline{\text{OE}} = V_{IL}$	_	-	450	ns
Output Enable to Output Delay	toE	$\overline{\text{CE}} = V_{IL}$	ovabita žauto	1 20 To v	120	- ns
Output Enable High to Output Float *	tor	$\overline{\text{CE}} = V_{IL}$	0	-	100	ns
Address to Output Hold	toн	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	TOARA	O DATH	ns.

^{*} tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:

Input Rise and Fall Times:

Output Load:

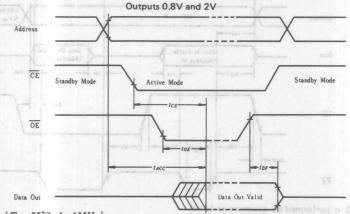
Reference Level for Measuring Timing:

177L Gate + 100oF 0.8V to 2.2V

≤ 20ns 5 5ns V8.0 ; atuquut

1TTL Gate + 100pF

Inputs 1V and 2V



• CAPACITANCE $(Ta=25^{\circ}C, f=1MHz)$

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance (Except $\overline{\text{OE}}/V_{PP}$)	GNI	V _{IN} =0V	Forestones a	AUR C. A. A. A.	6	pF
OE/V _{PP} Input Capacitance	C _{4 N2}	$V_{IN} = 0 \text{ V}$	-	-	20	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}$	-	-113	12	pF

PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS ($V_{cc} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$, $Ta = 25^{\circ}C \pm 5^{\circ}C$)

Parameter 7 + 60 0	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	$V_{IN} = 5.25 \text{V} / 0.4 \text{V}$	_	0.5heR	10	μA
Output Low Voltage During Verify	Vol	$I_{OL}=2.1\mathrm{mA}$	_	"oge " oV	0.4	tound VII
Output High Voltage During Verify	V _{OH}	$I_{OH} = -400 \mu\text{A}$	2.4	T -	- 12	and VV
Vcc Supply Current	Icc			_	150	m A
Input Low Level	VIL		-0.1	NOT7	0.8	JASV.
Input High Level (All Input Except $\overline{\text{OE}}/V_{PP}$)	VIH	PRISTICS (Ter) to	2.0	D SHETA	Vcc+1	V
VPP Supply Current	IPP	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{PP}$	_		30	m A

• AC PROGRAMMING CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$, $Ta = 25^{\circ}C \pm 5^{\circ}C$)

	and the second s	and the second second second second	W. D. Warden and P. P. S. Marrier and P. C. Warden.	and the second s	September 19 Septe	Secretary to demand	
An DI P	arameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time		tas	33 164	2	- (v	fonst ell re	μs
OE Setup Time		toes	30 104	2	-	avito Al Ja	μs
Data Setup Time	- 1.0-	tos	J.W.	2	-	Pacific V	μs
Address Hold Time	- 0,8	t _{AH}	Vin	0	_	specific (μs
OE Hold Time		t OEH	Voc. Loc	2		easileV we	μs
Data Hold Time	1.5	t DH	Ves Low	2	_	easileV da	μs
Chip Enable to Outpu	t Float Delay*	tor	SULTE WORK	0	S CALVES AND	120	ns
Data Valid from CE	7.0000	tov	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{IL}$	0017	DOLTON	1	μs
CE Pulse Width Duri	ing Programming	t pw	Symbol .	45	50	55	ms
OE Pulse Rise Time	During Programming	t _{PRT}	EF mal	50	-culat	togs e 0 o	ns
VPP Recovery Time		t vR	36 m.1	2	_	tout-Delay	μs

^{*} tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level:

Input Rise and Fall Times:

Output Load:

Reference Level for Measuring Timing:

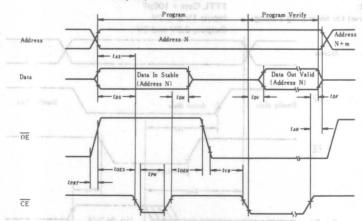
0.8V to 2.2V and modelness factories made and advention stagent and other in trade

≤ 20ns

1TTL Gate + 100pF

Inputs; 1V and 2V, O VO.0

Outputs; 0.8V and 2V



• ERASE

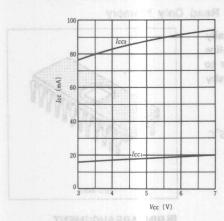
Erasure of HN462732 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this prosedure.

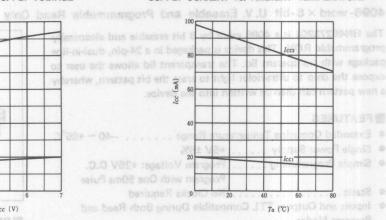
The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm².

CAPACITARCE (Ta-28°C, f-1MHz)



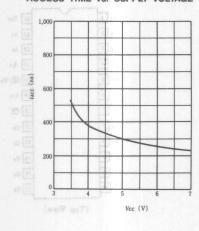
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

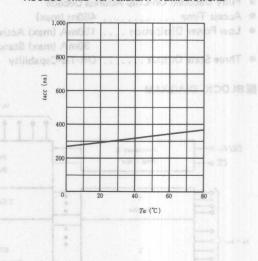




ACCESS TIME vs. SUPPLY VOLTAGE

ACCESS TIME vs. AMBIENT TEMPERATURE





HN462732GI

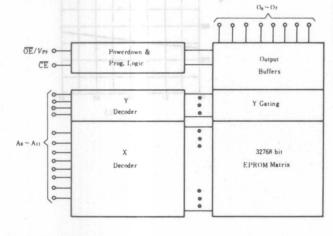
4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN462732GI is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

FEATURES

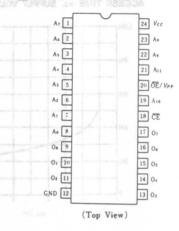
- Extended Operating Temperature Range −40 ~ +85°C
- Single Power Supply +5V ±5%
- Simple Programming Program Voltage: +25V D.C.
 Program with One 50ms Pulse
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time 450ns (max)
- Low Power Dissipation . . . 150mA (max) Active Currents
 30mA (max) Standby Current
- Three State Output OR-Tie-Capability

BLOCK DIAGRAM



(DG-24B)

PIN ARRANGEMENT



MODE SELECTION

Pins	CE (18)	OE /V _{PP} (20)	Vcc (24)	Outputs (9~11, 13~17)
Read	VIL	VIL	+5	Dout
Stand by	VIH	Den't Care	+5	High Z
Program	VIL	V_{PP}	+5	Din
Program Verify	VIL	VIL	+5	Dout
Program Inhibit	VIH	V _{PP}	+5	High Z

MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	O sant Tete today?	-65 to +125	°C
All Input and Output Voltage*	1785.28V.	-0.3 to +7	Input LeanVe Corsent
V _{PP} Voltage*	OE /VPP	-0.3 to +28	Cotput LawVeitage Dry

* With respect to GND

READ OPERATION

• DC AND OPERATING CHARACTERISTICS ($Ta = -40 \text{ to} + 85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$,)

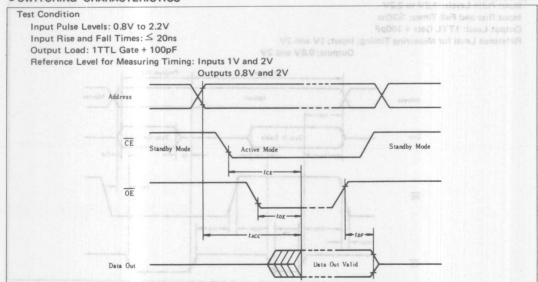
Parameter Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current (Except $\overline{\text{OE}}/V_{PP}$)	I_{LI1}	$V_{IN}=5.25\mathrm{V}$	-	-	10	μΑ
OE/VPP Input Leakage Current	ILIZ	$V_{IN} = 5.25 \mathrm{V}$	-	-	10	μA
Output Leakage Current	ILO	$V_{out} = 5.25 \text{V}/0.45 \text{V}$	REPORTE	MO 4/4	10	μA
Vcc Current (Standby)	Icci	$\overline{\text{CE}} = V_{IH}, \overline{\text{OE}} = V_{IL}$	-	801-70-01	30	m A
Vcc Current (Active)	Iccz	$\overline{OE} = \overline{CE} = V_{IL}$	-	-	150	m A
Input Low Voltage	VIL		-0.1	-	0.8	V
Input High Voltage	VIH		2.0	-	V _{cc} +1	V
Output Low Voltage	Vol	$I_{OL}=2.1\mathrm{mA}$	-	- 1	0.45	V
Output High Voltage	V _{OH}	$I_{OH} = -400 \mu\text{A}$	2.4	-		V

• AC CHARACTERISTICS (Ta = -40 to +85°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Condition	HN462732GI			Unit
			min.	typ.	max.	Ollit
Address to Output Delay	tACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	- goza	lone h gr 5 S	450	ns
CE to Output Delay	t _{CE}	$\overline{\text{OE}} = V_{IL}$	gallating 1	deing-Prop	450	ns
Output Enable to Output Delay	toE	$\overline{\text{CE}} = V_{IL}$		-	150	ns
Output Enable High to Output Float*	tDF	$\overline{\text{CE}} = V_{IL}$	0	glue Wards	130	ns
Address to Output Hold	t _{OH}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0		-	ns

^{*} tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS



• CAPACITANCE $(Ta=25^{\circ}C, f=1MHz)$

				and the second		
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance (Except $\overline{\text{OE}}/V_{PP}$)	Gni	V _{IN} -0V	Helselo Bus	HE DON LA	6	pF
OE/V _{PP} Input Capacitance	CINZ	V _{IN} -0V	utt vill s		20	pF
Output Capacitance	Cont	Vout - 0 V	Specimen.	WOOD TO A	12	pF

PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS ($V_{cc} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$, $T_a = 25^{\circ}C \pm 5^{\circ}C$)

Symbol	Test Condition	min.	typ.	max.	Unit
Iu	$V_{IN} = 5.25 \text{V} / 0.4 \text{V}$	_	*egame7	10	μΑ
Vol	$I_{OL}=2.1\mathrm{mA}$	_	_	0.4	sheVV N
V _{OH}	$I_{OH} = -400 \mu\text{A}$	2.4	_	0949 -0 0 35	V
Icc		_	94017	150	m A
VIL	RISTICS (TA = -40 to	-0.1	o aum	0.8	V
V _{IH}	Symbol	2.0	asioman	$V_{cc}+1$	V
IPP	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{PP}$	OE Need	os tall n	30	m A
	I LI VOL VOH ICC VIL VIH	I_{LL} $V_{IN} = 5.25 \text{V}/0.4 \text{V}$ V_{OL} $I_{OL} = 2.1 \text{ mA}$ V_{OH} $I_{OH} = -400 \mu\text{A}$ I_{CC} V_{IL} V_{IH}	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

TO ASSOLUTE MAXIMUM RATINGS

• AC PROGRAMMING CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$, $T_a = 25^{\circ}C \pm 5^{\circ}C$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	tas	30 324	2	-	setto <u>li</u> n	μs
OE Setup Time	toes		2		Va <u>ll</u> age	μs
Data Setup Time	tos	63	2		Vollage	μs
Address Hold Time	t _{AH}	Va. lus	0	-	egath <u>o</u> V s	μs
OE Hold Time	toen	V ₁₀₀ - V ₂₀₀	2		Salis C	μs
Data Hold Time	t _{DH}	10 +85°C, Pec = 5V = F	2	STACE	RACTER	μs
Chip Enable to Output Float Delay*	tor		0	_	120	ns
Data Valid from CE	tov	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{IL}$	_	- 20	1	μs
CE Pulse Width During Programming	t pw	(Acc CE+OE=F	45	50	55	ms
OE Pulse Rise Time During Programming	t _{PRT}	TOR OF YEL	50	-	valoG-ter	ns
VPP Recovery Time	t vr	tos CE-Fir	2	ipu+Delay	aO ot s ida	μs

^{*} tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

SWITCHING CHARACTERISTICS

Test Conditions Input Pulse Levels: 0.8V to 2.2V Input Rise and Fall Times: ≤20ns Output Load: 1TTL Gate + 100pF Reference Level for Measuring Timing: Input; 1V and 2V Outputs; 0.8V and 2V Program Verify Program Address Address Address Data In Stable Data Out Valid -tos-OE tpw. CE

• ERASE

Erasure of HN462732 is performed by exposure to Ultraviolet light of 2537A, and all the output data are changed to "1" after this prosedure.

The minimum integrated close (i.e., UV intensity x exposure time) for erasure is $15W \cdot \sec/cm^2$

HN482732AG-20, HN482732AG-25, HN482732AG-30

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN482732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.

The transparent lid on the package allow the memory content to be erased with ultraviolet light.

FEATURES

Single Power Supply +5V ±5%

• Simple Programming Program Voltage: +21V D.C

Program with one 50ms Pulse

Static..... No clocks Required

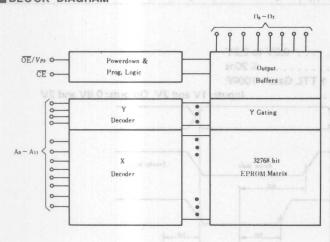
 Inputs and Outputs TTL Compatible During Both Read and Program Mode

Absolute Max. Rating of Vpp Pin . . . 26.5V

Low Stand-by Current 35mA (max)

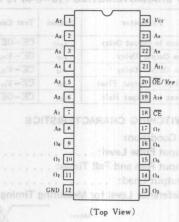
Compatible with Intel 2732A

■ BLOCK DIAGRAM



(DG-24B)

PIN ARRANGEMENT



■ MODE SELECTION

Pins	CE (18)	\overline{OE}/V_{PP} (20)	Vcc (24)	Outputs (9~11, 13~17)
Read	VIL	VIL	+5	Dout
Stand by	V_{IH}	Don't Care	+5	High Z
Program	VIL	VPP	+5	Din
Program Verify	VIL	VIL	+5	Dout
Program Inhibit	V_{IH}	VPP	+5	High Z

MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tats	-65 to +125	°C
All Input and Output Voltages*	Vin, Vout	-0.3 to +7	V
VPP Voltage *	OE/V _{PP}	-0.3 to $+26.5$	V
Vcc Voltage*	Vcc	-0.3 to +7	V

^{*} with respect to GND

READ OPERATION

• D.C. AND OPERATING CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±5%)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	Iu	V _{IN} =5.25V	_	_	10	μΑ
Output Leakage Current	ILO	$V_{out} = 5.25 \mathrm{V}$	_	_	10	μ A
Vcc Current (Standby)	Iccı	$\overline{\text{CE}} = V_{IH}, \ \overline{\text{OE}} = V_{IL}$	(8+ m)	Tioù	35	mA
Vcc Current (Active)	Iccz	$\overline{OE} = \overline{CE} = V_{IL}$	6x4 -	<u> </u>	150	mA
Input Low Voltage	VIL	action with one signs Pulsa	-0.1	-	0.8	V
Input High Voltage	V_{IH}	hasing 9 resolu	2.0	_	Vcc+1	V
Output Low Voltage	Vol	IoL=2.1mA	Commission		0.45	V
Output High Voltage	V on	$I_{OH} = -400 \mu\text{A}$	2.4	_		V

● AC CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±5%)

Parameter Symb	Cb.1	nbol Test Conditions	HN4827	HN482732AG -20		HN482732AG -25		HN482732AG-30	
rarameter			min	max	min	max	min	max	Unit
Address to Output Delay	tACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$		200	.03	250	10 50 185	300	ns
CE to Output Delay	tcE	$\overline{\text{OE}} = V_{IL}$	_	200	00	250	10350	300	ns
OE to Output Delay	t OE	$\overline{\text{CE}} = V_{IL}$	10	90	10	100	10	150	ns
OE High to Output Float	tor	$\overline{\text{CE}} = V_{IL}$	0	80	0	90	0	130	ns
Address to Output Hold	t on	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	_	0	-	0	NOAMS)	ns

• SWITCHING CHARACTERISTICS

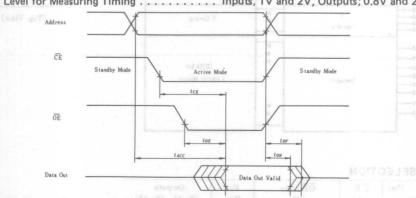
Test Conditions

Input Pulse Level: 0.8V to 2.2V

 Input Rise and Fall Times:
 ≤ 20ns

 Output Load:
 1 TTL Gate + 100PF

Reference Level for Measuring Timing Inputs, 1V and 2V, Outputs; 0.8V and 2V



• CAPACITANCE ($Ta = 25\,^{\circ}\text{C}, \ f = 1\,\text{MHz})$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance (Except $\overline{\mathrm{OE}}/V_{PP}$)	CINI	$V_{IN}=0$ V			6	pF
OE /VPP Input Capacitance	C _{IN2}	V _{IN} =0 V			20	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}$			12	pF

■ PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS ($T_a = 25 \text{ °C} \pm 5 \text{ °C}$, $V_{cc} = 5 \text{ V} \pm 5 \text{ %}$, $V_{PP} = 21 \text{ V} \pm 0.5 \text{ V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	$V_{IN} = V_{IL}$ or V_{IH}	_	100-10	10	μΑ
Output Low Voltage During Verify	Vol	IoL=2.1mA	rst3-,t	JU Hid	0.4	V
Output High Voltage During Verify	V _{OH}	$I_{OH} = -400 \mu\text{A}$	2.4	1018-63	487.584	V
Vcc Supply Current	Icc	seckaged to a 22 oin dual-in	derica i	ald T.M	150	mA
Input Low Level	VIL	an with an fell to suppose the	-0.1	tos to dar	0.8	V
Input High Level (All Inputs Except $\overline{\text{OE}}/V_{PP}$)	V_{IH}	soluli enteriumatu alabu beng	2.0	tastano y	Vcc+1	V
V _{PP} Supply Current	IPP	$\overline{\text{CE}} = V_{IL}, \ \overline{\text{OE}} = V_{PP}$			30	mA

• AC PROGRAMMING CHARACTERISTICS ($Ta=25\,^{\circ}\text{C}\pm 5\,^{\circ}\text{C}$, $V_{cc}=5\text{V}\pm 5\,\%$, $V_{PP}=21\text{V}\pm 0.5\text{V}$)

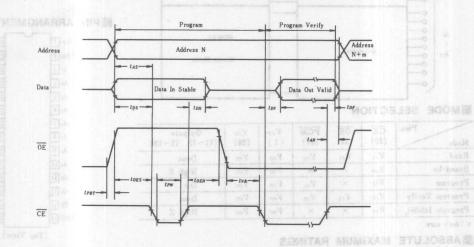
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Address Setup Time	tas	Program with one ours	2	-	-	μs
OE Setup Time	toEs	BATT ENDOED BYLL	2	10-11	1 1 1	μs
Data Setup Time	tos	sus hash ning burn hash and	2	1 1 2144	UU Dille	μs
Address Hold Time	t_{AH}		0		forle,	μs
OE Hold Time	t OEH	HN452764/G 250N	2	4 4 - 4 1	aras I	μs
Data Hold Time	t DH	HNAB2764/9-3 300m	2		-	μs
Chip Enable to Output Float Delay*	t _{DF}	HN482784/G-4 450ns	0	_	130	ns
Data Valid from CE	t _{DV}	$\overline{\text{CE}} = V_{IL}, \ \overline{\text{OE}} = V_{IL}$	edimas	gor fl so	307 1 1 19	us
CE Pulse Width During Programming	t _{PW}	Arabb	45	50	55	ms
OE Pulse Rise Time During Programming	t _{PRT}		50	Clean it	aliw e ld ies	ns
V _{PP} Recovery Time	t vR	0-0	2	-		μs

^{*} toF defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Condition

Reference Level for Measuring Timing: Inputs 1V and 2V; Outputs 0.8V and 2V



• ERASE

Erasure of HN482732A is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm².

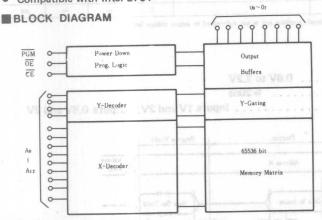
HN482764, HN482764-3, HN482764-4, HN482764G, HN482764G-3, HN482764G-4

8192-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

FEATURES

- Simple Programming Program Voltage: +21V D.C.
 Program with one 50ms Pulse
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- High Performance Programming Available
- Compatible with Intel 2764



MODE SELECTION

Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	Vcc (28)	Outputs (11~13, 15~19)
Read	VIL	VIL	VIH	Vcc	Vcc	Dout
Stand-by	V_{IH}	×	×	Vcc	Vcc	High Z
Program	V_{IL}	×	VIL	V_{PP}	Vcc	Din
Program Verify	V_{IL}	V_{IL}	VIH	V_{PP}	Vcc	Dout
Program Inhibit	V_{IH}	×	×	V _{PP}	Vcc	High Z

^{× :} don't care

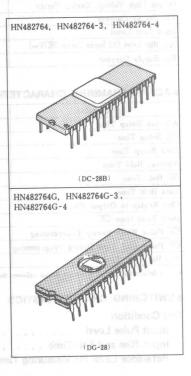
BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value of 6	Unit
Operating Temperature Range	Topr	0 to +70	Jan C 11
Storage Temperature Range	Tets	-65 to +125	°C
All Input and Output Voltage*	V _τ	-0.3 to +7	V
V _{PP} Voltage	V_{PP}	-0.3 to $+26.5$	V

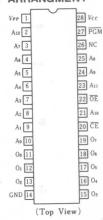
^{*:} with respect to GND

328





PIN ARRANGMENT



READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5$ V $\pm 5\%$, $V_{PP}=V_{cc}\pm 0.6$ V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	ILI	$V_{CC} = 5.25 \text{V}, \ V_{in} = 5.25 \text{V}$	_		10	μA
Output Leakage Current	ILO	$V_{cc} = 5.25 \mathrm{V}, \ V_{out} = 5.25 \mathrm{V} / 0.4 \mathrm{V}$	<u> 2</u> 31%	PF 30 <u>17</u> 50	10	μA
V _{PP} Current	I_{PP1}	$V_{PP} = V_{CC} + 0.6 \mathrm{V}$	7/10	N SHITEG	15	m A
Vcc Current (Standby)	Icc 1	$\overline{\text{CE}} = V_{IH}$		- L	35	m A
Vcc Current (Active)	Iccz	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$		100	150	m A
Input Low Voltage	VIL	219	-0.1		0.8	V
Input High Voltage	V_{IH}	for [Ob =PGB = V _G	2.0	-	$V_{cc}+1$	V
Output Low Voltage	Vol	$I_{OL}=2.1\mathrm{mA}$	-	-	0.45	V
Output High Voltage	Von	$I_{OH} = -400 \mu\text{A}$	2.4	10 A	EMARI20	V

• AC CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5$ V $\pm 5\%$, $V_{PP}=V_{cc}\pm 0.6$ V)

Parameter	Symbol	Test Conditions	HN482	2764/G	HN4827	764/G-3	HN4827	764/G-4	Unit
	Symbol	Test Conditions	min max	max	min	max	min	max	
Address to Output Delay	g tACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	unt -	250	-	300	-	450	ns
CE to Output Delay	t _{CE}	$\overline{OE} = V_{IL}$	202	250	_	300	and said	450	ns
OE to Output Delay	t oe	$\overline{\text{CE}} = V_{IL}$	10	100	10	150	10	150	ns
OE High to Output Float	t _{DF}	$\overline{\text{CE}} = V_{IL}$	0	90	0	130	0	130	ns
Address to Output Hold	tон	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	-	0	_	0	Carlo F July	ns

Note: tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:

Input Rise and Fall Time:

Output Load:

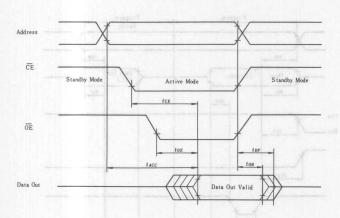
Reference Level for Measuring Timing:

0.8V to 2.2V ≤ 20ns

1TTL Gate + 100pF

Inputs; 1V and 2V

Output; 0.8V and 2.0V



• CAPACITANCE ($Ta=25^{\circ}C$, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	-	4	6	pF
Output Capacitance	Cout	$V_{\text{out}} = 0 \text{ V}$	ed fagersor	8	12	pF

PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=5V±5%, Vpp=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	ILI	$V_{in} = 5.25 \mathrm{V}$	-		10	μΑ
Output Low Voltage During Verify	Vol	$I_{OL}=2.1\mathrm{mA}$	-		0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400 \ \mu \text{A}$	2.4	-	- 10	V
Vcc Current (Active)	Iccz	-W-35		_	150	m A
Input Low Level	VIL	N = S(N = N)	-0.1		0.8	V
Input High Level	V_{IH}		2.0		$V_{cc}+1$	V
VPP Supply Current	I_{PP}	$\overline{\text{CE}} = \overline{\text{PGM}} = V_{IL}$	-		30	m A

• AC PROGRAMMING CHARACTERISTICS ($Ta=25\%\pm5\%$, $V_{cc}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$)

Parameter	Symbol Test Condition		min	typ	max	Unit
Address Setup Time	tas	the state of the same of	2	ele uri a le	ing a keep	μs
OE Setup Time	toes		2	_	_	μs
Data Setup Time	tos	John Tage Codern	2	-	Parame	μ_{S}
Address Hold Time	tan		0			μs
Data Hold Time	t _{DH}	LIV = AV = RV DAV	2	-K413	a vidamin d	μs
OE to Output Float Delay	tor	10s 10s = Viu	0		130	ns
VPP Setup Time	tvs	194 - 107 - 107	2		veleU_tiel0	μs
PGM Pulse Width During Programming	tpw	154 OE=1715	45	50	55	ms
CE Setup Time	tces	10g [CE = DE = V _E	2		ANGED IN	μs
Data Valid from OE	toE	to mediants are a summary and	ildno ipolov	MES (15 <u>EC</u>) 23	150	ns

Note: tof defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:

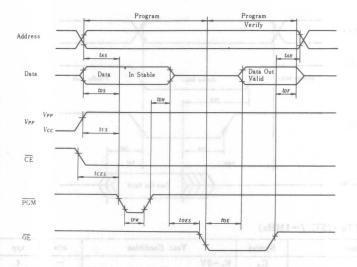
Input Rise and Fall Time:

Reference Level for Measuring Timing:

0.8V to 2.2V ≤ 20 ns

Input; 1V and 2V

Output; 0.8V and 2V

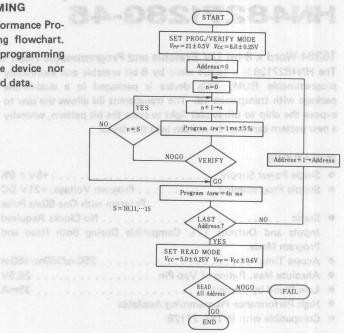


ERASE

Erasure of HN482764 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W · sec/cm²

HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

• AC PROGRAMMING CHARACTERISTICS $(T_a=25\,^{\circ}\text{C}\pm5\,^{\circ}\text{C},\ V_{cc}=6\text{V}\pm0.25\text{V},\ V_{PP}=21\text{V}\pm0.5\text{V})$

Parameter	Symbol	Test Condition	mi n	typ	max	Unit
Address Setup Time	tas	EUMTUS	2	0103 MAC 0		μs
OE Setup Time	toes		2	-	-	μs
Data Setup Time	tos		2		-	μs
Address Hold Time	t _{AH}	OMPAS V	0	guillo Turi.	-	μs
Data Hold Time	t _{DH}		2	-	-	μs
OE to Output Float Delay*	tor		0		130	ns
V _{PP} Setup Time	t vps		2	_	-	μs
Vcc Setup Time	t vcs		2	-	-	μs
PGM Pulse Width during Initial Program	t _{PW}	AN AGUNAN	0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	topw		3.8	-	63	ms
CE Setup Time	tces		2		-	μs
Data Valid from OE	t OE		-	-	150	ns

* tDF defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. ** torw is defined as mentioned in flort chart.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:

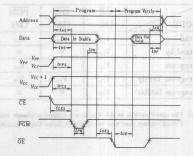
0.8V to 2.2V

Input Rise and Fall Time:

 \leq 20 ns

Reference Level for Measuring Timing: Input; 1V and 2V

Output; 0.8V and 2V





HN4827128G-25, HN4827128G-30, HN4827128G-45

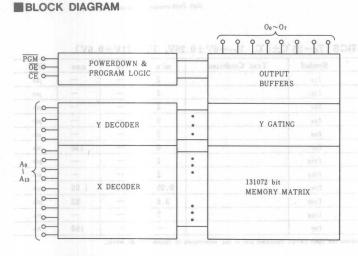
16384-Word x 8-bit UV Erasable and Programmable Read Only Memory

The HN4827128 is a 16384 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

FEATURES

-	LATORES
	Single Power Supply
•	Simple Programming Program Voltage: +21V DC
	Program with One 50ms Pulse
	Static No Clocks Required
	Inputs and Outputs TTI Compatible During Both Read and

- High Performance Programming Available
 Compatible with INTEL 27128
- _____



(DG-28)

PIN ARRANGEMENT



MODE SELECTION

Pins	CE (00)	ŌĒ	PGM	V_{PP}	Vcc	Outputs
MODE	(20)	(22)	(27)	(1)	(28)	(11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	Vcc	Vcc	Dout
Stand by	V_{IH}	×	×	Vcc	Vcc	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	Vcc	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{cc}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{cc}	High Z

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.

MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	Topr	lodene 0 to +70	°C
Storage Temperature Range	Tets Ves 3	-65 to +125	Input Le Dige Cerre
All Input and Output Voltages*	VIN, Vout	-0.3 to +7	Output LVs Voltage
V _{PP} Voltage*	V_{PP}	-0.3 to +26.5	Ostput HVA Voltage
Vcc Voltage*	Vcc	-0.3 to +7	Var CorrVat (Active

^{*} with respect to GND

READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm5\%$, $V_{PP}=V_{cc}\pm0.6V$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	V _{cc} =5.25V, V _{IN} =5.25V		its Tale	10	μΑ
Output Leakage Current	I_{LO}	V _{CC} =5.25V, V _{out} =5.25V/0.4V	- I	-500	10	μΑ
V _{PP} Current	I_{PP1}	$V_{PP} = V_{CC} + 0.6V$	-	1-	5 T 5	mA
Vcc Current (Standby)	I_{cc1}	$\overline{\text{CE}} = V_{IH}$		_	35	mA
Vcc Current (Active)	I_{cc2}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	60	100	mA
Input Low Voltage	V_{IL}	The second secon	-0.1	-	0.8	V
Input High Voltage	V_{IH}	912	2.0	elatt an	$V_{cc}+1$	V
Output Low Voltage	V_{OL}	I _{OL} =2.1mA		-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400 \mu A$	2.4	nistel e	HIJV VIIII	V

• AC CHARACTERISTICS (Ta=0 to 70°C, $V_{cc}=5V\pm5\%$, $V_{PP}=V_{cc}\pm0.6V$)

Parameter	Symbol	Test Condition	HN4827	HN4827128G-25		HN4827128G-30		HN4827128G-45	
rarameter	Symbol	Test Condition	min	max	min	max	min	max	Unit
Address to Output Delay	tACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	250	_	300	- :	450	ns
CE to Output Delay	t _{CE}	$\overline{OE} = V_{IL}$	VAO	250	_	300	Ings.J.	450	ns
OE to Output Delay	t OE	$\overline{\text{CE}} = V_{IL}$	85>	100	_	120	all Total	150	ns
OE High to Output Float	t _{DF}	$\overline{\text{CE}} = V_{IL}$	0	85	0	105	0	130	ns
Address to Output Hold	t on	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	-	0	_	0	_	ns

^{*} IDF defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:

0.8V to 2.2V

Input Rise and Fall Time:

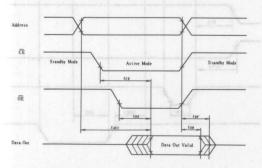
≤ 20 ns

Output Load:

1 TTL Gate + 100 pF

Reference Level for Measuring Timing: Inputs; 1V and 2V

Outputs; 0.8V and 2.0V



• CAPACITANCE ($Ta=25^{\circ}C$, f=1 MHz)

Parameter	Symbol	Test Condition	min typ		max	Unit
Input Capacitance	Cin	Vin=0V - 544500000 54458	19 17.11	4	6	pF
Output Capacitance	Cout	V _{out} =0V	(1.) <u>e</u> lon	8	12	pF

PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS $(Ta=25^{\circ}\text{C}\pm5^{\circ}\text{C}, V_{cc}=5\text{V}\pm5\%, V_{PP}=21\text{V}\pm0.5\text{V})$

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25 \text{V}$		tur u Ra	10	μΑ
Output Low Voltage During Verify	V_{OL}	I _{OL} =2.1mA	****	of A l- nog	0.45	V
Output High Voltage During Verify	V _{OH}	$I_{OH} = -400 \mu A$	2.4	_	7 10 0	VV
Vcc Current (Active)	Iccz	1 Nos	_	_	100	mA
Input Low Level	V_{IL}		-0.1	- 0	0.8	V
Input High Level	V_{IH}		2.0	-	$V_{cc}+1$	V
VPP Supply Current	I_{PP}	$\overline{\text{CE}} = \overline{\text{PGM}} = V_{IL}$	-1	OFTAF	30	mA

• AC PROGRAMMING CHARACTERISTICS $(Ta=25^{\circ}C\pm5^{\circ}C, V_{cc}=5V\pm5\%, V_{PP}=21V\pm0.5V)$

Parameter Parameter	Symbol	Test Condition	14	min	typ	max	Unit
Address Setup Time	tas	Vcc-5,25V, Vac-5,25V0.4	ral.	2	37 44 183	egl <u>ul</u> es.	μs
OE Setup Time	toes	V += V2c+0.8Y	Link	2		4557	μs
Data Setup Time	t _{DS}	CE+ Vis	lest	2	<u>"d</u> bus	18) <u>Inst</u>	μs
Address Hold Time	t _{AH}	CE-08-16	stol-	0	<u>L</u> =2/(1	W. Jan	μs
Data Hold Time	t _{DH}		7,14	2	_ 9	estlaŭ e	μs
OE to Output Float Delay	t _{DF}		- 4/4	0	_ 8	130	ns
V _{PP} Setup Time	t vs	Am 1 . 2 - 20 k	10.7	2	-034	sin/_ve_	μs
PGM Pulse Width During Programming	t _{PW}	Au,003 m2	Ho	45	50	55	ms
CE Setup Time	t ces			2	_	_	μs
Data Valid from OE	t OE	10°C. No-2773- NA-	at Dest	200	SILST.	150	ns

Note: tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Condition

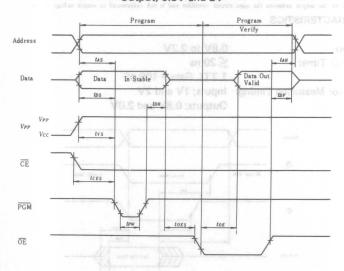
Input Pulse Level:

Input Rise and Fall Time:

0.8V to 2.2V < 20 ns

Reference Level for Measuring Timing: Input; 1V and 2V

Output; 0.8V and 2V

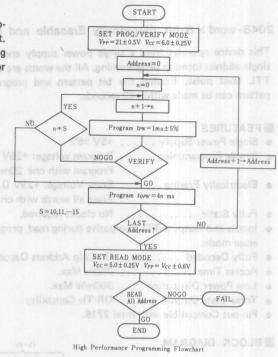


• ERASE

Erasure of HN4827128 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W·sec/cm2.

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flow chart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



• AC PROGRAMMING CHARACTERISTICS ($Ta=25^{\circ}\text{C}\pm5^{\circ}\text{C}$, $V_{CC}=6\text{V}\pm0.25\text{V}$, $V_{PP}=21\text{V}\pm0.5\text{V}$)

Parameter	Symbol	Test Condition	on	min	typ	max	Unit
Address Setup Time	tas	Section and		2		<u>F</u> 31	μs
OE Setup Time	toes		- April 1990	2	_	-0 -1	μs
Data Setup Time	t _{DS}			2		-	μs
Address Hold Time	t _{AH}			0	- 1	- +	μs
Data Hold Time	t DH			2	- 1	-0-	μs
OE to Output Float Delay*	t _{DF}		-	0		130	ns
VPP Setup Time (AV (5)T)	t vps			2	- 1		μs
Vcc Setup Time	t vcs	56 \$855		2	- 1	0 1	μs
PGM Pulse Width during Initial Program	t _{PW}	SUMMI ACTRICAL		0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	t _{OPW}		W	3.8	-1	63	ms
CE Setup Time	tces			2	-	-01	μs
Data Valid from OE	t OE		J L.	-		150	ns

^{*} tDF defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:

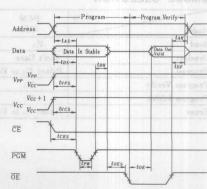
Input Rise and Fall Time:

Reference Level for Measuring Timing: Input; 1V and 2V

0.8V to 2.2V

< 20 ns

Output; 0.8V and 2V



^{**} topw is defined as mentioned in flow chart.

HN48016P

2048-word × 8-bit Electrically Erasable and Programmable ROM

This device operates from a single power supply and features fast single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new months of the pattern of notific here. pattern can be made within 42 seconds.

FEATURES

Single Power Supply +5V ±5%

Simple Programming Program voltage: +25V D.C.

Program with one 20ms pulse.

Electrically Erasing Erase Voltage: +25V D.C.

Erase all words with one 200ms pulse.

Fully Static No clocks required.

Inputs and Outputs TTL compative during read, program and erase mode.

Fully Decoded On-Chip Address Decode.

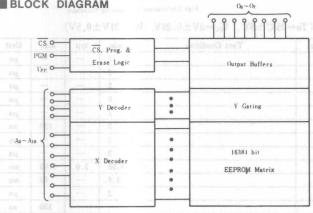
Access Time 350ns Max.

Low Power Dissipation 300mW Max.

Three State Output OR-Tie Capability

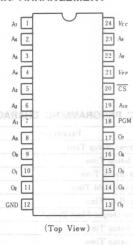
Pin-out Compatible with Intel 2716.

■ BLOCK DIAGRAM





PIN. ARRANGEMENT



MODE SELECTION

Pins	PGM (18)	CS (20)	V _{PP} 30 (21)	(24)	Outputs (8~11, 13~17)
Read	VIL	VIL	+5	+5	Dout
Deselect	Don't Care	VIH	+5	+5	High Z
Program	Pulsed VIL to VIH	VIH	+25	+5	Din
Program Verify	VIL	VIL	+25	+5	Dout
Program Inhibit	VIL	ViH	+25	+5	High Z
Erase	Pulsed VIL to VIH	VIL	+25	+5	High Z

B ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
All Input and Output Voltage	VIN, Vout	-0.3 to $V_{CC} + 0.3$ or $V_{PP} + 0.3$	V
Vcc Voltage	Vcc	-0.3 to +7.0	V.
V _{PP} Voltage	V_{PP}	-0.3 to +28	V
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tstg	-55 to +125	°C

READ OPERATION

• DC AND OPERATING CHARACTERISTICS ($V_{cc}=5$ V $\pm5\%$, $V_{PP}=V_{cc}\pm0.6$ V,* Ta=0 to $+70^{\circ}$ C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	ILI	V _{IN} =5.25 V	_	-	10	μΑ
Output Leakage Current	ILO	$V_{OUT} = 5.25 \mathrm{V}$	_		10	μΑ
Vcc Current	Icc1	$\overline{\mathrm{CS}} = V_{IH} / V_{IL}$		32	50	m A
V _{PP} Current	I _{PP1}	V _{PP} =5.85 V		4	7 0	m A
34 -	VIL	sud	-0.1		0.8	V
Input Voltage	V_{IH}	nel	2.0	_	3 <u></u> T	V
80 100 08	V _{OL}	I _{OL} = 1.6 m A	χ a(<u></u>)	sold-by-	0.4	V
Output Voltage	V _{OH}	$I_{OH} = -100 \mu\text{A}$	2.4	tein a	0.00 01 30	V

^{*} The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.

• AC CHARACTERISTICS ($V_{cc}=5V\pm5\%$, $V_{PP}=V_{cc}\pm0.6V$, $T_a=0$ to $+70^{\circ}$ C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address to Output Delay	tacc	$PGM = \overline{CS} = V_{IL}$		200	350	ns
Chip Select to Output Delay	tco	$PGM = V_{IL}$		70	150	ns
Chip Deselect to Output Float	tor	The state of the s	0	40	100	ns
Address to Output Hold	toн	$PGM = \overline{CS} = V_{IL}$	10			ns

• TEST CONDITION

Input pulse levels:

Input rise and fall time:

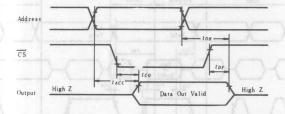
Output load:

Reference level for Measuring Timing:

0.8V to 2.0V

≦ 20ns

1TTL Gate + 100 pF Inputs 1V and 1.8V Outputs 0.8V and 2.0V



• CAPACITANCE ($Ta=25^{\circ}C$, f=1MHz)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0 \text{ V}$	-	7.5	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}$		15	pF

PROGRAM OPERATION

• DC PROGRAMMING CHARACTERISTICS ($V_{cc} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$, $T_a = 0$ to +70°C)

Parameter	4.50.8	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	0.0-0	Iu	$V_{IN} = 5.25 \mathrm{V}$			10	μΑ
Vcc Supply Current	8,0-	Iccz	100	_	32	50	m A
VPP Supply Current	0	I _{PP2}	Mark Mark		10	20	m A
1 128 - 1 1 1 2 1 1	32-	V_{IL}	7.00	-0.1	Ruger	0.8	V
Input Voltage		V_{IH}		2.0	_	_	V

● AC PROGRAMMING CHARACTERISTICS (V_{CC} = 5V±5%, V_{PP} = 25V±1V, T_d = 0 to +70℃)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	tas	V25 2-5N 1 13	2	100	Sage Cura	μs
CS Setup Time	tcss	V30.2************************************	2	- 491	College Col	μs
Data Setup Time	tos	Jon Carling Va	2	-	1616	μs
Address Hold Time	t _{AH}	June Varieties	2*	_	- 301	μs
CS Hold Time	tcsH	N.	7	-	-	μs
Data Hold Time	t _{DH}	150	2	_	_000	μs
Chip Deselect to Output Float Delay	tor	Voc 1 for = 1.5mA	0	40	100	ns
Chip Select to Output Delay	tco	Via 160 - 100 nA		70	150	ns
Program Pulse Width	tew	all our philades to have a	15	20	25	ms
Program Pulse Rise Time	tPRT		5	_	_	ns
Program Pulse Fall Time	tpft		5	_	_	ns
VPP Setup Time (D'07+	O tps	1 ± 596, Vee = Vec ± 0, 6	10	BOIT IA	ITO AND	μs
V _{PP} Hold Time	tрн		10	_		μs
CS to Program Mode Time	tvs	NOT CONTROL	10		100.00	μs
VPP Read Mode Time	t vH	(F) 75 G J = 15 D 3 (1)	10	Em at	TRADEC 91	μs

• TEST CONDITION

Test Condition

Input pulse levels: Input rise and fall time:

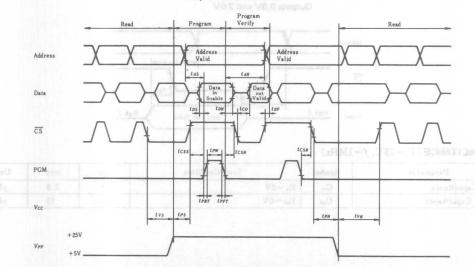
Reference level for Measuring Timing:

0.8V to 2.0V V0.\$ or V8.0

20ns (10% to 90%)

Input; 1V and 1.8V

Output: 0.8V and 2.0V



ERASE OPERATION

• DC ERASING CHARACTERISTICS ($V_{cc}=5V\pm5\%$, $V_{PP}=25V\pm1V$, $T_a=0$ to +70%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	ILI	$V_{IN} = 5.25 \mathrm{V}$	-		10	μΑ
Vcc Supply Current	Iccs		138979 - 1447	32	50	m A
VPP Supply Current	I _{PP3}		(c)((i)) 10	10	20	m A
7 . 77 1.	VIL	- lancon	-0.1		0.8	V
Input Voltage	VIH		2.0	7	-	V

• AC ERASING CHARACTERISTICS ($V_{cc}=5V\pm5\%$, $V_{PP}=25V\pm1V$, $T_a=0$ to +70°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
CS Setup Time	tecss		2	6069	-	μs
PGM to Output Delay	tEO		7	-		μs
Erase Pulse Width	t EW		190	200	210	ms
Erase Pulse Rise Time	tert		5	-	-	ns
Erase Pulse Fall Time	teft		5	-	BUSATTERS	ns
VPP Setup Time	tes	door 99 V Vd	10	Carego XI	3511,2101,0	μs
VPP Hold Time	t _{EH}	edity ,asono	10	N 994 Vs	S ,Descele	μs
Erase Program Time t_{EP}	t _{EP}	daīn, keep thn	10	I 1562/10 0	T -,62010 E	μs
Program Enase Time tpE	t PE	bas enoted au	10	1.6.10 ¹ "W	ELL, FE ME	μs

• TEST CONDITION

Test Condition

Input pulse levels:

Input rise and fall time:

Reference level for Measuring Timing:

0.8V to 2.0V 20ns (10% to 90%)

Input; 1V and 1.8V
Output; 0.8V and 2.0V

POWER SUPPLY SEQUENCE PRECAUTIONS

To protect the written data, power supply to the HN48016P should be turned on and off in the following order:

Power On-Off Order and Input Level Limitation for CS and PGM Terminals

Table 1 shows the relationship between the order in which power supply for the HN48016P should be turned on and off and the input levels of the $\overline{\text{CS}}$ and PGM terminals.

- (1) For the 5V V_{PP} and V_{CC}, there is no limitation as to the order in which power is turned on and off the state of the input terminals CS and PGM.
- (2) When turning on and off power supply for the 25V Vpp, keep V_{CC} at between 4.5V and 7V, and PGM at "Low."
- (3) When turning on and off power supply for the 5V V_{CC} while V_{PP} equals 25V ± 1V (this being a rare case for the HN48016P), make sure to keep PGM at "Low."

Fig. 1 shows the timing order in which power is a bound as an analysis and turned on and off.

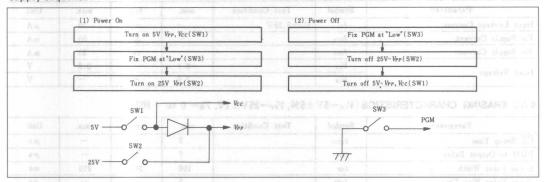
Table 1. Power On-Off Order for HN48016P

Input Level		Powe	r On-Off		
PGM	CS	5V- V _{PP} - V _{CC}	25 V- V _{PP}		
V_{IL}	VIL	Possible	Possible only whe		
VIL	V_{IH}	Possible	$V_{cc} = 4.5 \sim 7 \text{V}^{*2}$		
V_{IH}	VIL	Possible	impossible*2		
VIH	VIH	Possible	impossible		

- Note 1. If Power for the 25V Vpp were turned on or off while V_{CC} = -0.3V to +4.5V, the data holding characteristic would probably deteriorate.
- Note 2. If the 25V Vpp were operated to choose a "write" or "erase" mode while PGM = "V_{IH}," contents of ROM would probably change.

Example of Standard Power Supply Sequence

The following is an example of standard power supply sequence:



Inter-mode Timing

The HN48016P has six operating modes, 5V V_{PP} readout, non-selected, 25V V_{PP} write, write check, write inhibit, and erase. To protect the written data, keep the terminal PGM at "Low" for a period of 10µs before and after turning the terminal V_{PP} from 5V to 25V and vice versa.

The following describes the inter-mode timing for a system that uses the HN48016P.

■ Readout → Write → Readout

Before turning the terminal V_{PP} to 25V, keep the terminal PGM at "Low" for a period of 10µs minimum (as indicated by t_{VS}). After the terminal V_{PP} has been turned to 25V, keep the terminal CS at "Low" for a period of 10µs minimum (as indicated by t_{PS}). Before turning the terminal V_{PP} to 5V, keep the terminal CS at "Low" for a period of 10µs minimum (as indicated by t_{PH}). After the terminal V_{PP} has been turned to 5V, keep the terminal PGM at "Low" for a period of 10µs minimum (as indicated by t_{VH}).

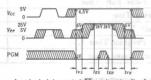
Readout→Erase → Readout

This timing sequence is shown in Fig. 3. After turning the terminal V_{PP} to 25V, keep the terminal PGM at "Low" for a period of 10 μ s minimum (as indicated by tes). Keep the terminal PGM at "Low" for a period of 10 μ s minimum (as indicated by teh) before turning the terminal V_{PP} to 5V, as well.

● Erase → Write → Erase

This timing sequence is shown in Fig. 4. Before turning the terminal \overline{CS} to "High (write mode)," keep the terminal.

PGM at "Low" for a period of 10μ s minimum (as required by tep). Before turning from "write" to "erase," keep the terminal \overline{CS} at "Low" for a period of 10μ s minimum (as indicated by tep).



Input level of the terminal CS may be either "Lo or "High" $tvs = t\varepsilon s = t\varepsilon n = tvn \ge 10 \mu s$

Fig. 1. Power on-off timing sequence.

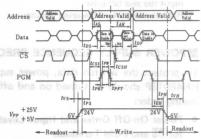


Fig. 2. "Readout → Write → Readout" timing

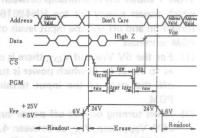


Fig. 3. "Readout → Erase → Readout" timing.

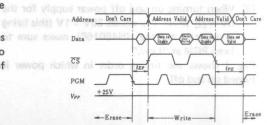


Fig. 4. "Erase→Write→Erase" timing.



HMIO414, HMIO414-1

256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access namory developed for high speed systems such as setaton pad and control/buffer storages.

The fabrication process uses the Histori's law capacitance, exide isolation marked on the double contalination.

The MILIDATA is exceptulated in cerdip-TSpin package, compatible with Fairchild's 510414.

- hand 109 MOL Arive elektromen with 8 M
- Address access time: HM10414t 10ns (mex.)
- 1 9mm1 = 68 1 A12 G1 MH
 - Write pulse width: Sec (min.)
 - e Three chip select pins
- Catput obtainable by wired-OR (open emitter)

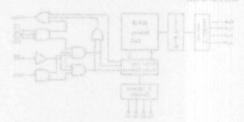


M PIN ARRANGEMENT



BIBAT HTURTS

		×		II are go		
Write "9"	a l	1				
Write "1"				-		
b4521	BIP					
			PS PS			
				meve		



COMPTAIN DEBMIYANA STREETSCHAFF

-55 to 4 125	F.ac(Blue)"	

self volet 5

HM10414, HM10414-1

256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

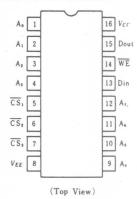
- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.)

HM10414-1: 8ns (max.)

- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)

(DG-16)

PIN ARRANGEMENT

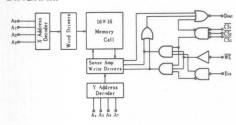


TRUTH TABLE

		Input		0-11	M.J.	
C	3	WE	Din	Output	Mode	
any o	ne H	×	×	L	Not Selected	
all	L	L	L	L	Write "0"	
all	L	L	H	L	Write "1"	
all	L	Н	×	Dout *	Read	

- ×: Don't care
- * : Read out non-inverted

BLOCK DIAGRAM



MASSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to VEE	V
Output Current	Lout	-30	mA
Storage Temperature	Tets	-65 to +150	°C
Storage Temperature	Tets (Bias)*	-55 to +125	°C

^{*} Under Bias

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE} = -5.2 \text{V}$, $R_L = 50 \Omega$ to -2.0 V, Ta = 0 to $+75 ^{\circ}\text{C}$, air flow exceeding 2 m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
	TENER		0°C	-1000	-	-840	
	V _{OH}	70.0-	+25°C	-960		-810	
Output Voltage			+75°C	-900		-720	17
		$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1870		-1665	mV
	Vol	N ver-	+25°C	-1850	- 1	-1650	
		1-14	+75°C	-1830	- , -	-1625	
Cos sys	12000		0°C	-1020		-	N. Harris
	V.onc		+25°C	-980	-		e/0.0
			+75°C	-920	-1.	-	mV GA39
Output Threshold Voltage		$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	_986	- 18	-1645	
	Volc	(=91874)	+25°C	Shifter (Lett)	- (4.5	-1630	
			+75°C	-		-1605	
			0°C	-1145		-840	mV
	V_{IH}	Guaranteed Input Voltage	+25°C	-1105	-	-810	
		High for All Inputs	+75°C	-1045		-720	
Input Voltage	+=173==		0°C	-1870	A 18.	· -1490	
	VIL	Guaranteed Input Voltage	+25°C	-1850	-	-1475	
		Low for All Inputs	+75°C	-1830	a tradition of the	-1450	
	IIH	$V_{IN} = V_{IHA}$	0 to +75°C		-	220	
Input Current		CS		0.5		170	μA
and the second s	IIL	$\begin{array}{ c c c c c }\hline Other & V_{IN} = V_{ILB} \\ \hline \end{array}$	0 to +75°C	-50		3021	STINK
The second second	-	All Input and Output Open,	+75°C	1 =00	-130	图 -	
Supply Current	IEE	Test Pin 8	0°C	-180	-140	-	m A

• AC CHARACTERISTICS

 $(V_{EE} = -5.2 \text{V} \pm 5\%, T_a = 0 \text{ to } +75^{\circ}\text{C}, \text{ air flow exceeding 2m/sec, see test circuit and waveforms})$

1. READ MODE

7.	C. 1.1	Test Condition		HM 1041	1	ŀ	IM 10414	-1	Unit
Item	Symbol	lest Condition	min	typ	max	min	typ	max	Onit
Chip Select Access Time	tACR	V.		3	6		3	6	ns
Chip Select Recovery Time	tres	1	101-4	3	6	-	3	6	ns
Address Access Time	taa	4) <u></u> -y \-	7	10		6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	$t_{WSA} = 2 \text{ ns}$	6	4		ns
Data Setup Time	twsp		1	0	1991/01	ns
Data Hold Time	twhD	V 280 0	4812 1 MA	0	NA 22	ns
Address Setup Time	twsA	tw=6ns	2	0		ns
Address Hold Time	twhA		2	0	H	ns
Chip Select Setup Time	twscs		1	0		ns
Chip Select, Hold Time	twncs		1	0	-	ns
Write Disable Time	tws		-	T	5	ns
Write Recovery Time	twR			-	5	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t,	a l	-	1.5	2.5	ns
Output Fall Time	t_f			1.5	2.5	ns

4. CAPACITANCE

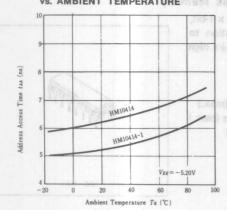
Item State	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin		-	3	5	pF
Output Capacitance	Cout		-	5	8	pF

TEST CIRCUIT AND WAVEFORMS - T. VO.S- at 108- 31.75.8- - 21.8017219370ARAMO DO 4 2. INPUT PULSE 1. LOADING CONDITIONS GND -0.9V -15 -20% HM10414 RL \ $t_r = t_f = 2.0$ ns typ 0.01µF -2.0V 0 $R_L = 50\Omega$ VEE $C_L = 30 \text{pF} (\text{includes jig and stray capacitance})$ 3. READ MODE 50% Address - 50% cs -t ACS--t 4.4-80% Dout 4. WRITE MODE CS 50% P AC CHARACTERISTICS Address 50% L twin 50% WE t wsa-Dout SUPPLY CURRENT SUPPLY CURRENT vs. SUPPLY VOLTAGE VS. AMBIENT TEMPERATURE 160 160 mA) IEE 140 120 120 100 100 $V_{EE} = -5.20V$ Ta=25°C -5.72 100 20 40 60 -5 20

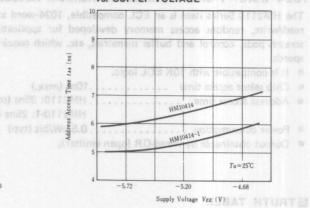
Supply Voltage VEE (V)

Ambient Temperature Ta (°C)

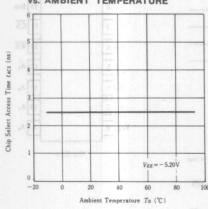
ADDRESS ACCESS TIME



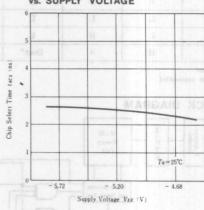
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE 1991 BEST A MODIFIE Vs. SUPPLY VOLTAGE



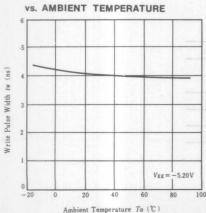
CHIP SELECT ACCESS TIME VS. AMBIENT TEMPERATURE



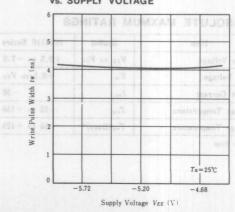
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



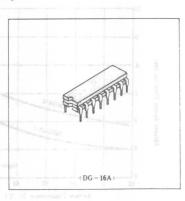
HM2110, HM2110-1

1024-word×1-bit Fully Decoded Random Access Memory Management 1028-1000 Access Memory Memory

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.

- Power consumption , 0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).

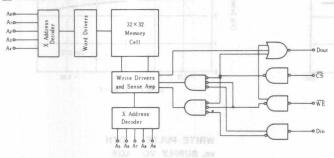


TRUTH TABLE

	Input	0	M - 1		
CS	WE	Din	Output	Mode	
Н	× 3a	(X Y)	ans ar	Not Selected	
L	L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout*	Read	

- ×: irrelevant
- * : Read out noninverted

BLOCK DIAGRAM



PIN ARRANGEMENT

Dout	1		16	١
A _o	2		15] [
Aı	3		14	1
Az	4		13	Į
As	5		12]
Α.	6		11	1
As	7		10	1
VEE	8		9	1

■ ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	$+0.5$ to V_{EE}	V
Output Current	Iout	-30	mA
Storage Temperature	Tstg	-65 to +150	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

* Under Bias



■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-5.2$ V, $R_L=50\Omega$ to -2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
an		- 1	0°C	-1000	l.:	-840	#4 204am
	V_{OH}		+25°C	-960	-	-810	
			+75°C	-900		-720	CAPAC
Output Voltage	111	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1870	-	-1665	mV
70	Vol		+25°C	-1850	-	-1650	
Tr. 3 1			+75°C	-1830	-	-1625	
			0°C	-1020			NECTE:
	Vonc		+25°C	-980	ANIA_ :	UUNIU	
0		2.JUR TURKE S	+75°C	-920	20	10407 9	LOVDIN
Output Threshold Voltage		$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	-		-1645	mV
Z	Volc		+25°C	-	317-41	-1630	
1805-1		1	+75°C	-	-	-1605	
	Library Comments		0°C	-1145	+	-840	
107.40	V_{IH}	Guaranteed Input Voltage High for All Inputs	+25°C	-1105		-810	
1 1 1		righ for All Inputs	+75°C	-1045	3 4	-720	
Input Voltage			0°C	-1870	1 +	-1490	mV
	VIL	Guaranteed Input Voltage Low for All Inputs	+25°C	-1850	L -	-1475	
		Low for All Inputs	+75°C	-1830	-2.0	-1450	
	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	-	DOTAL TOTAL	220	Jan 1997
Input Current	7	\overline{CS} $V_{IN} = V_{ILB}$	0 +- 175°C	0.5	10 - 10 <u>-</u>	170	μΑ
	I_{IL}	Other	0 to +75°C	-50	_	-	
Supply Current	1	All Input and Output Open,	0 ≤ Ta < 25°C	-150	-100	340N	READ
Supply Current	IEE	Test Pin 8	<i>Ta</i> ≥ 25°C	-125	-90	1-	mA

• AC CHARACTERISTICS

 $(V_{EE} = -5.2 \text{V} \pm 5\%, Ta = 0 \text{ to } +75^{\circ}\text{C}, \text{ air flow exceeding 2m/sec, see test circuit and waveforms})$

1. READ MODE

Item	Symbol	Test Condition		HM2110			HM2110 -	1	Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs		-	7	10	-	7	10	ns
Chip Select Recovery Time	t RCS			7	10	/	7	10	ns
Address Access Time	tAA		_	20	35	7	15	25	ns

2. WRITE MODE

market to on the	C 11	Trans Carling	HM2110			HM2110-1			Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	tw	$t_{WSA} = 8 \text{ns}$	25		-	25	-	_	ns
Data Setup Time	twsp		5	102	-	5	-	-	ns
Data Hold Time	twHD		5	pa I =	-	5	-	3.0	ns
Address Setup Time	twsA	$t_W=25\mathrm{ns}$	8			8	_	_	ns
Address Hold Time	twha	1 V	2		-	2	-		ns
Chip Select Setup Time	twscs	111/2	5	-	-	5	-	_	ns
Chip Select Hold Time	twncs		5	-	_	5	_	_	ns
Write Disable Time	tws		_	-	10	-	-	10	ns
Write Recovery Time	twR		_	-	10	_	_	10	ns

3. RISE/FALL TIME

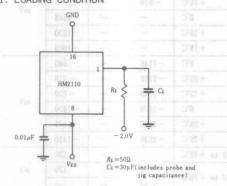
sealing Item, example	Symbol	Test Condition	min ?	typ	max	Unit O
Output Rise Time	t.	Test s'andrian	-	5	- 110	ns
Output Fall Time	t,	No.		5		ns

4. CAPACITANCE

Item	Symbol	Test	Condition	min	typ	max	Unit
Input Capacitance	Cin	785+		-	4	5	pF
Output Capacitance	Cout	1789 1		_	7	8	pF

TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

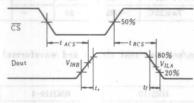


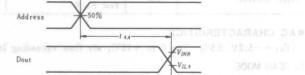
2. INPUT PULSE



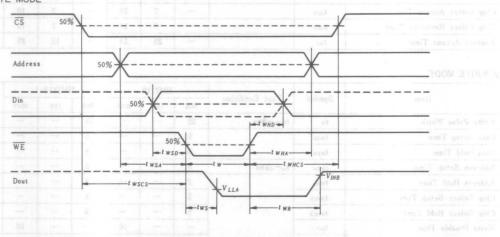
 $t_r = t_I = 2.5$ ns typ

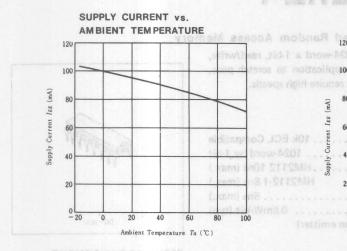
. 3. READ MODE

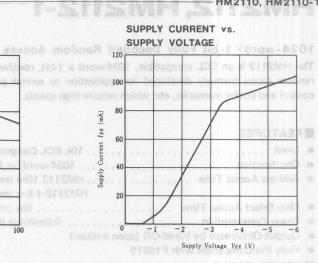


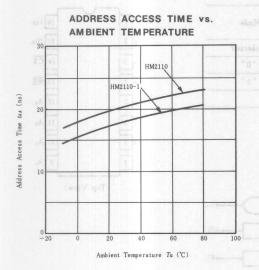


4. WRITE MODE











HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

FEATURES

- Construction 1024-word by 1-bit

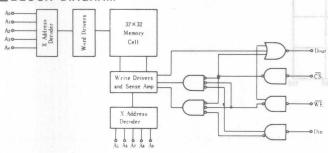
- Power Consumption 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

TRUTH TABLE

Mode	0		Input	
Mode	Output	Din	WE	CS
Not Selected	L	×	×	Н
Write "0"	L	L	L	L
Write "1"	L	Н	L	L
Read	Dout*	×	Н	L

- × : Irrelevant
- * : Read out noniverted

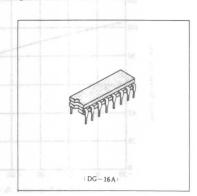
BLOCK DIAGRAM



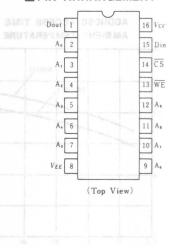
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	VEE to VCC	+0.5 to -7.0	V
Input Voltage	Vin	$+0.5$ to V_{EE}	V
Output Current	Iout	-30	mA
Storage Temperature	Tstg	-65 to +150	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

^{*} Under Bias



PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

 $(V_{EE} = -5.2\text{V}, R_L = 50\Omega \text{ to } -2.0\text{V}, Ta = 0 \text{ to } +75^{\circ}\text{C}, \text{ air flow exceeding } 2\text{m/sec})$

• DC CHARACTERISTICS

Item	Symbol	Test Condition	1	min(B)	typ	max(A)	Unit
	8 3 6		0°C	-1000	-	-840	
	V_{OH}		+25°C	-960	_	-810	L CAPAC
neU ann a d		Comilities min	+75°C	-900	_	-720	.,,
Output Voltage	+ 12.5	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1870		-1665	mV
19 8	Vol		+25°C	-1850	_	-1650	Output O
			+75°C	-1830	-	-1625	
			0°C	-1020	MA 11	WHIL	0.0213
	Vonc 3	2. NPUT PUL	+25°C	-980	110	10/10/12	HOAD.L.
		VEN-	+75°C	-920	_	UISO I	.,
Output Threshold Voltage	5. BH	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	_	-	-1645	mV
	Volc	T	+25°C	-	-	-1630	
			+75°C	polonika.	1-	-1605	
ge) 110.5	m, a		0°C	-1145	-	-840	
	V_{IH}	Guaranteed Input Voltage High for All Inputs	+25°C	-1105	1-1-	-810	
Y		High for All Inputs	+75°C	-1045	l	-720	
Input Voltage			0°C	-1870	-	-1490	mV
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	+25°C	-1850	-	-1475	Tutto
		Low for All Inputs	+75°C	-1830	ruk -	-1450	
	IIL	$V_{IN} = V_{IHA}$	0 to +75°C	erbeind 23 et	-0 -	220	
Input Current		CS	0 . 175°C	0.5	_	170	μΑ
	IIL	$V_{IN} = V_{ILB}$ Other	0 to +75°C	-50	-	-	What d
C 1 C	7	All Input and Output Open,	Ta = 0°C	-200	-	,	
Supply Current	IEE	Test Pin 8	<i>Ta</i> = 75°C	-170	1177-7	-	mA

• AC CHARACTERISTICS

 $(V_{EE} = -5.2 \text{V} \pm 5\%, Ta = 0 \text{ to } +75^{\circ}\text{C}, \text{ air flow exceeding 2m/sec, see test circuit and waveforms})$

1. READ MODE

Thom	Symbol	Test Condition		HM2112-	1		HM2112	SCHOOL ST	Unit
Item	Symbol	lest Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs		1	3	5	1/	3	5	ns
Chip Select Recovery Time	trcs		1 1	3	5	1	3	5	ns
Address Access Time	taa	parenta	3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	S	Test Condition	1	HM2112-	1		HM2112		11.4
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 3$ ns	6	2		6	2		ns
Data Setup Time	twsp	rout Armen	1	0	-	1	0	37	ns
Data Hold Time	t wh D		1	0	-	1	0	-	ns
Address Setup Time	twsa	$t_{w}=6$ ns	3	0	010 90	3	0	silvili.	ns.
Address Hold Time	t wha		2	0	-	2	0	-	ns
Chip Select Setup Time	twscs		1	0	-	1	0	-	ns
Chip Select Hold Time	t whc s		1	0	-	1	0	-	ns
Write Disable Time	tws		1	3	5	1	3	- 5	ns
Write Recovery Time	twn		1	3	5	1	3	5	ns

3. RISE/FALL TIME

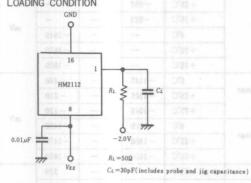
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t,		0.8	1.5	2.5	ns
Output Fall Time	t _j		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	1.14.1	1	3	5	pF
Output Capacitance	Cout		3	5	8	pF

TEST CIRCUIT AND WAVEFORMS





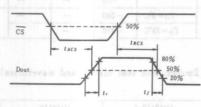
2. INPUT PULSE

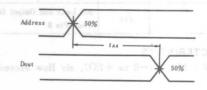




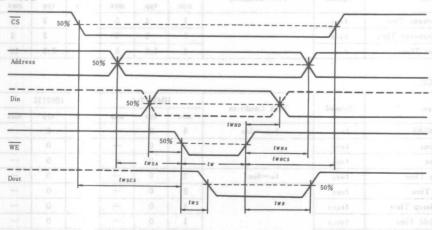
 $t_r = t_f = 2.0 \text{ms} \text{ typ}$

3. READ MODE

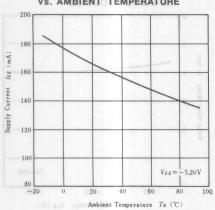




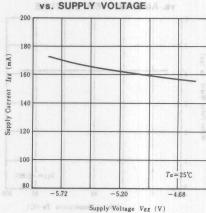
4. WRITE MODE



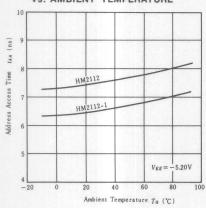
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



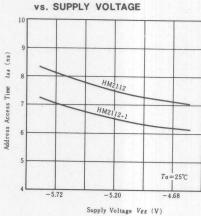
SUPPLY CURRENT



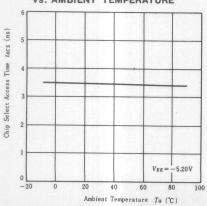
ADDRESS ACCESS TIME
vs. AMBIENT TEMPERATURE



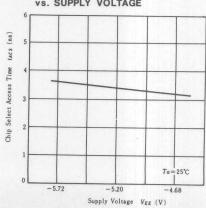
ADDRESS ACCESS TIME



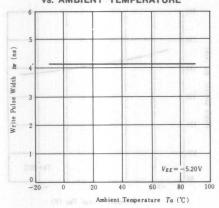
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



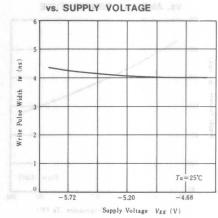
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



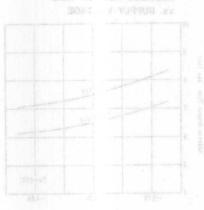
WRITE PULSE WIDTH
vs. AMBIENT TEMPERATURE



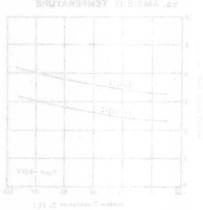
WRITE PULSE WIDTH



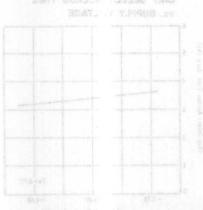
ADDRESS ACC IS TIME



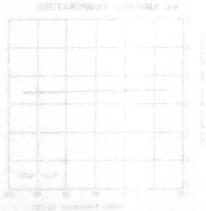
ADDRESS ACCESS THRE



CHIP SELECT NOCESS TIME



ONIP SHURET ACCESS THAT



HM10422

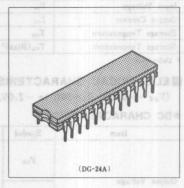
256-word×4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.



FEATURES

- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

PIN ARRANGEMENT

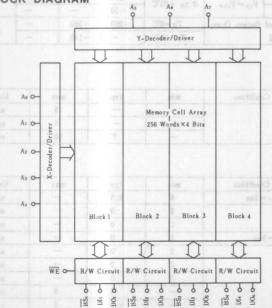


TRUTH TABLE

OSSI Input			+ 25°C	
BS	WE	Din	Output	Mode
Н	×	×	L	Not Selected
L	L	L	L L	Write "0" MA
VaL 0	L	Н	L L	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant

* : Read out noninvert BLOCK DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
nput Voltage	Vin	$+0.5$ to V_{EE}	V
Output Current	Iout	-30	mA
Storage Temperature	Tets	-65 to +150	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

^{*} Under Bias

■ ELECTRICAL CHARACTERISTICS

 $(V_{EE}=-5.2\text{V},~R_L=50\Omega~\text{to}~-2.0\text{V},~T_a=0~\text{to}~+75^{\circ}\text{C},~\text{air flow exceeding }2\text{m/sec})$

• DC CHARACTERISTICS

Item	Symbol	Test Condit	on	min(B)	typ	max(A)	Unit
			0°C	-1000	_	-840	ZEE-w ZEE-w Vm ¹ V Addre
tas-bu	V_{OH}	V_{OH} $V_{IN} = V_{IHA}$ or V_{ILB}	+25°C	-960		-810	
			+75°C	-900	the state of the	-720	
Output Voltage			0°C	-1870	C EURINE UN	-1665	
THEMBOMASH	Vol		+25°C	-1850	Q1 -9 <u>11</u> 112	-1650	
-			+75°C	-1830	Listin Tun	-1625	White
Output Threshold Voltage	135/		0°C	-1020	MC.V_IC	D 8 d1887 0-	JANO.
	Vonc		+25°C	-980	W VG_BIO	801834 <u>0</u> 3	mV
		,, ,, ,, ,,	+75°C	-920	_	_	
	190	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	_		-1645	
	Volc		+25°C	_	- 101	-1630	
1214 [02]		Mode	+75°C	Tile		-1605	
*RJ (81	70		0°C	-1145	-	-840	T.
(30 81)	V_{IH}	Guaranteed Input Voltage	+25°C	-1105	_	-810	
		High for All Inputs	+75°C	-1045		-720	
Input Voltage	14	1 83/17/	0°C	-1870		-1490	mV
	VIL	Guaranteed Input Voltage	+25°C	-1850	- 1	-1475	.1
W/BI		Low for All Inputs	+75°C	-1830	_	-1450	1) = tas
-ph 342 Ap-	IIH	$V_{IN} = V_{IHA}$	0 to +75°C	-		220	20 1 20
Input Current	W.	BS	0 1 75°0	0.5	MAIR	170	μΑ
	I_{IL}	$\begin{array}{ c c c c c }\hline Other & V_{IN} = V_{ILB} \\ \hline \end{array}$	0 to +75°C	-50	_	_	
(Top Figure		All Input and Output Ope	$Ta = 0^{\circ}C$	-200	-160	-	
Supply Current	I_{EE}	Test Pin 12	$Ta = 75^{\circ}C$	· -	-145	_	mA

• AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	M Unit
Block Select Access Time	tabs		parié lisz grandi	_	5	ns
Block Select Recovery Time	trbs		018 AX #10 W 272		5	ns
Address Access Time	taa		_	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 2$ ns	6	4.5	- 1	ns
Data Setup Time	twsp	Block (2	0	1 - 1	ns
Data Hold Time	t wh D		2	0	+ 1	ns
Address Setup Time	twsa	$t_w = 6$ ns	2	0	J -	ns
Address Hold Time	t wha		2	0	_	ns
Block Select Setup Time	twsss	SHOOL WAS THE	2	0		ns
Block Select Hold Time	t whbs		2	0	_	ns
Write Disable Time	t ws		0 0 0 0	4 0	5	ns
Write Recovery Time	t wR		日 日 日 日 日	4.5	9	ns

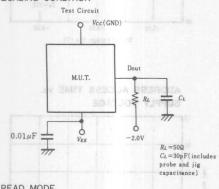
Item	Symbol	Test Condition	min 351	typ	max	Unit
Output Rise Time	t.	700	- 1	2	- T	ns
Output Fall Time	t _f			2		ns

4. CAPACITANCE

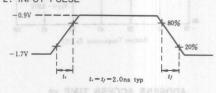
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	Lau A	-	4		pF
Output Capacitance	Cout			7		pF

TEST CIRCUIT AND WAVEFORMS

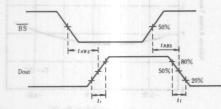
1. LOADING CONDITION

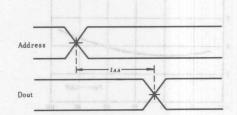


2. INPUT PULSE

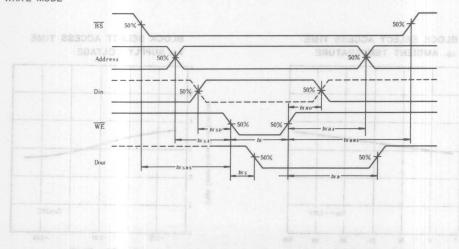


3. READ MODE

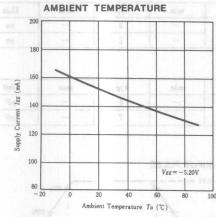




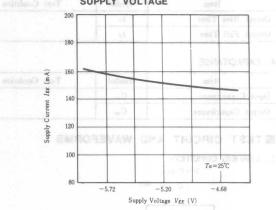
4. WRITE MODE



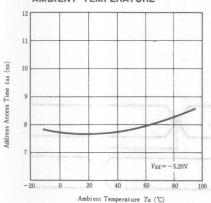
SUPPLY CURRENT vs.



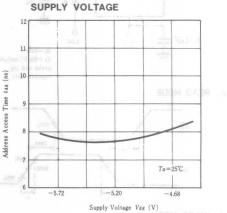
SUPPLY CURRENT vs. SUPPLY VOLTAGE



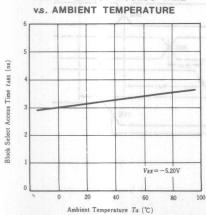
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



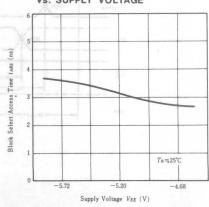
ADDRESS ACCESS TIME vs.

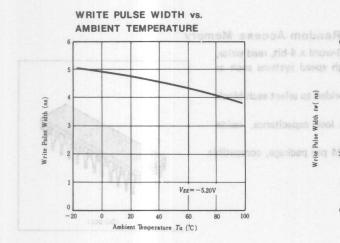


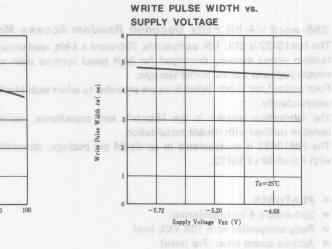
BLOCK SELECT ACCESS TIME



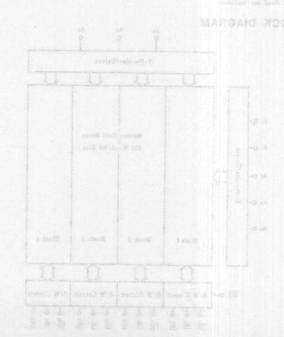
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE











HM10422-7

256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

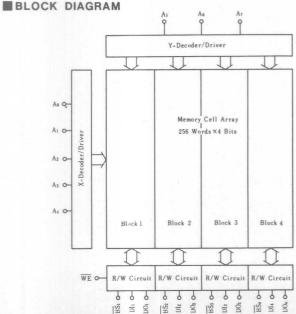
- FEATURES
- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

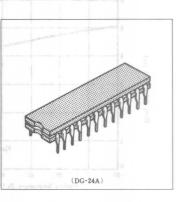
TRUTH TABLE

	Input	0	W 1	
BS	WE	Din	Output	Mode Not Selecte Write "0" Write "1" Read
Н	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

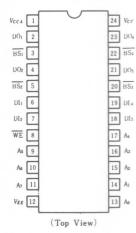
Notes) ×: Irrelevant
*: Read out noninvert

BU COK BIACBAN





■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V	
Input Voltage	Vin	+0.5 to VEE	V	
Output Current	Iout	-30	mA	
Storage Temperature	Tets	-65 to +150	°C	
Storage Temperature	Tstg (Bias)*	-55 to +125	°C	

^{*} Under Bias

■ ELECTRICAL CHARACTERISTICS

 $(V_{EE} = -5.2\text{V}, R_L = 50\Omega \text{ to } -2.0\text{V}, Ta = 0 \text{ to } +75^{\circ}\text{C}, \text{ air flow exceeding } 2\text{m/sec})$

• DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit	
	-		0°C	-1000	1100	-840		
	Von		+25°C	-960	QMD) SH	-810		
	27 100	$V_{IN} = V_{IHA}$	+75°C	-900	- 1	-720	mV	
Output Voltage		or VILB	0°C	-1870	-	-1665	m v	
	Vol		+25°C	-1850	-	-1650		
	4	3.	+75°C	-1830		-1625		
			0°C	-1020	-	_		
	Vonc		+25°C	-980	-	_	mV	
			+75°C	-920	-1	_		
Output Threshold Voltage	10 127	$-V_{IN} = V_{IHB}$ or V_{ILA}	0°C	0_	-0	-1645		
	Volc		+25°C	_	-101	-1630		
			+75°C		-	-1605		
			0°C	-1145		-840	D QA38	
	V_{IH}	Guaranteed Input Voltage	+25°C	-1105	-	-810		
		High for All Inputs	+75°C	-1045	-	-720		
Input Voltage			0°C	-1870	-	-1490	mV	
	V_{IL}	Guaranteed Input Voltage	+25°C	-1850	1	-1475	28	
		Low for All Inputs	+75°C	-1830		-1450		
THE RESERVE THE SECOND	IIH	$V_{IN} = V_{IHA}$	0 to +75°C		31-	220		
Input Current	1.	BS	0 / 750	0.5	17%-	170	μА	
	IIL	$V_{IN} = V_{ILB}$ Other	0 to +75°C	-50	1 -			
	-	All Input and Output Open,	Ta = 0°C	-240	-200			
Supply Current	I _{EE} Test Pin 12		<i>Ta</i> = 75°C	_	-180	2000	mA	

• AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	tABS				5	ns
Block Select Recovery Time	tras				5	ns
Address Access Time	taa	***	A	4	7	ns

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 2 \text{ ns}$	4	3	_	ns
Data Setup Time	twsp		1		-	ns
Data Hold Time	t wh D		1		- Un-	ns
Address Setup Time	twsa	$t_W = 4 \mathrm{ns}$	2		-	ns
Address Hold Time	t wha		1		-	ns
Block Select Setup Time	twsss		1		-	ns
Block Select Hold Time	t whbs		1		-	ns
Write Disable Time	tws		-	3	5	ns
Write Recovery Time	t wR			3	5	ns

3. RISE/FALL TIME

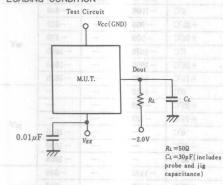
Item	Symbol	Test Condition	min min	typ	max	Unit
Output Rise Time	t.	V + 0.4-	a 2.04- 1 o	2	-	ns ns
Output Fall Time	t _f	Y Y s	1 1.0+ _	2	-	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin		-	3	_	pF
Output Capacitance	Cont		8 21 1.81	5	HU PAGE	pF

TEST CIRCUIT AND WAVEFORMS

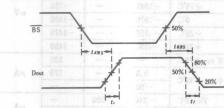
1. LOADING CONDITION

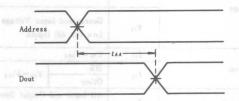


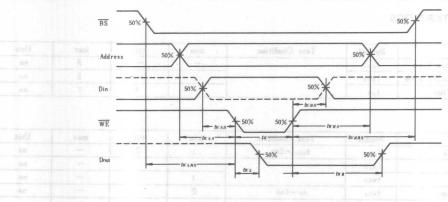
2. INPUT PULSE



3. READ MODE







HM10470, HM10470-1, HM10470F

4096-word x 1-bit Fully Decoded Random Access Memory
The HM10470/F is ECL 10K compatible, 4096-words x 1-bit, read
write random access memory developed for high speed systems such
as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470/F is encapsulated in cerdip-18 pin and Flat-18 pin package, compatible with Fairchild's F10470.

FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level

Address access time: HM10740/F 25ns (max)

HM10470-1 15ns (max)

Write pulse width: HM10470/F 25ns (min)

HM10470-1 15ns (min)

• Low power dissipation: 0,2mW/bit

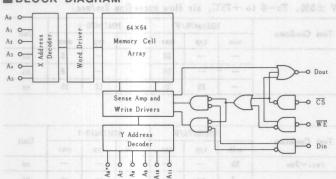
Output obtainable by wired-OR (open emitter)

TRUTH TABLE

	Input		Output	W.J. 9		
CS	WE	WE Din		WE Din		Mode
Н	×	× Not		Not Selected		
L	L	L	L	Write "0"		
L	L	Н	J'0=0 L	Write "1"		
L	Н	×	Dout*	Read		

Notes) × : Irrelevant * : Read Out Noninvert

■ BLOCK DIAGRAM

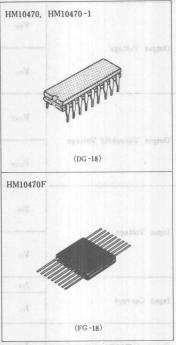


ABSOLUTE MAXIMUM RATINGS $(Ta=25^{\circ}C)$

Symbol	Rating	Unit	
VEE to Vcc	+0.5 to -7.0	V	
Vin	+0.5 to VEE	V	
Iout	-30	mA	
Tota	-65 to +150	°C	
Tsts (Bias)*	-55 to +125	°C	
	VEE to Vcc Vin Iout Toig	$V_{EE} \text{ to } V_{CC} +0.5 \text{ to } -7.0$ $V_{is} +0.5 \text{ to } V_{EE}$ $I_{out} -30$ $T_{sig} -65 \text{ to } +150$	

* Under Bias





PIN ARRANGEMENT



TEST CIRCUIT AND WAVEFORMS

•DC CHARACTERISTICS ($V_{EE} = -5.2\text{V}$, $R_L = 50\Omega$ to -2.0V, Ta = 0 to $+75^{\circ}\text{C}$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	etible, 4086	min (B)	typ	max(A)	Unit	
1-0100	113416478	doug ameteya boega	0°C	-1000	omun u ei	-840	toer edite	
	Von		+25°C	-960	eentroly	-810	a scraticini he febrie	
		citance, oxide Isola-	+75°C	-900	1 21 27270	-720		
Output Voltage		$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1870	m əld <u>u</u> əl	-1665	mV	
	Vol	oin and Elac-18 pin	+25°C	-1850	edeou.775	-1650		
Was -			+75°C	-1830	4 (12) V <u>.</u> 9)	-1625	1,586-35	
			0°C	-1020	_	_		
	Vonc		+25°C	-980	_	u rt es	TABS :	
		V - V V		-920	nsgro Ti d	T x t o os	mV	
Output Threshold Voltage		$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	OK BCL	€ d'v a d	-1645	- Fully	
(a(- \d)	Volc	(xem) at	+25°C	MH -	ः :सम्बंध	-1630	albbA 4	
	ness milit	er (mon)	+75°C	IMH -	_	-1605		
		(nim) as	0°C	-1145	1.099	-840	6717	
	VIH	Guaranteed Input Voltage	+25°C	-1105	_	-810		
		High for All Inputs		-1045	thelism	-720	d Mon	
Input Voltage			0°C	-1870	M. Act Blog	-1490	mV	
	VIL	Guaranteed Input Voltage	+25°C	-1850		-1475		
		Low for All Inputs	+75°C	-1830		-1450		
	ItH	$V_{IN} = V_{IHA}$	0 to +75°C	_	- 100	220	-	
Input Current		CS	0	0.5		170	μA	
	IIL	$V_{IN} = V_{ILB}$ Other	0 to +75°C	-50	-	-	H	
(94-1/3)		9 1011	m 0°0	-200*	-160*	-		
Supply Current	IEE	All Input and Output Open,	Ta = 0°C	-280**	-200**		mA	
		Test Pin 9	Ta=75°C		-145		1	

^{*} HM10470/F

•AC CHARACTERISTICS ($V_{EE} = -5.2\text{V} \pm 5\%$, Ta = 0 to $+75^{\circ}\text{C}$, air flow exceeding 2m/sec)

Item	Symbol Test Condition	Total Condition	HM10470/F			MM10470-1			Unit
		min	typ	max	min	typ	max	i onit	
Chip Select Access Time	tacs	100G S-0	-	_	10	16.779	-	8	ns
Chip Select Recovery Time	trcs		_ •	-	10	_	-	8	ns
Address Access Time	taa		_	15	25		12	15	ns

To any	C	Test Condition	HM10470/F			HM10470-1			Unit
Item W W	Symbol Test Condition		min	typ	max	min	typ	max	Unit
Write Pulse Width	ż w	twsA = 3ns	25	-	1-6	15	ķ —	_	ns
Data Setup Time	twsp		2	-	2.5	2	3	_	ns
Data Hold Time	t wh D		2	- - -	12.75 A 22	2	v - 11	0.013-14	ns
Address Setup Time	twsa	$t w = t w_{\min}$	3	7	0.17171	3	7177100	1.00	ns
Address Hold Time	t wha	7000	2		locare	2		n <u>er</u> 1	ns
Chip Select Setup Time	twscs		2	0+	to_Ver	2	-	<u> </u>	ns
Chip Select Hold Time	twncs	V 1 35	2		-	2	-	_936	ns
Write Disable Time	tws		_	_	10	red _		8	ns
Write Recovery Time	twr		- ut e	-	10	42	113	8	ns

^{**} HM10470-1

SUPPLY CURRENT VS.

3. RISE/FALL TIME

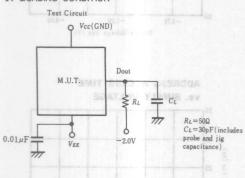
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.			2	- 43/8	ns
Output Fall Time	t,			2	-	ns

4. CAPACITANCE

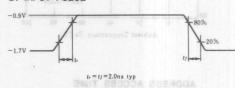
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	061		3		pF
Output Capacitance	Cout		and the same	5		pF

TEST CIRCUIT AND WAVEFORMS

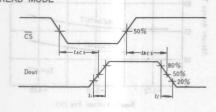
1. LOADING CONDITION

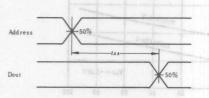


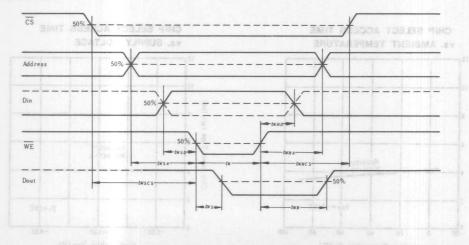
2. INPUT PULSE



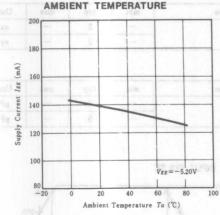
3. READ MODE



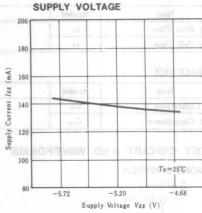




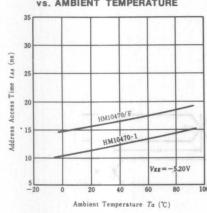
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



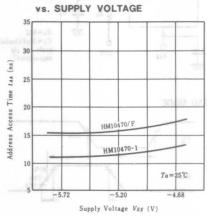
SUPPLY CURRENT VS. MAT LEAR 3281 .



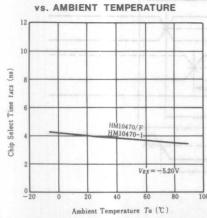
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



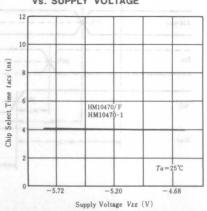
ADDRESS ACCESS TIME



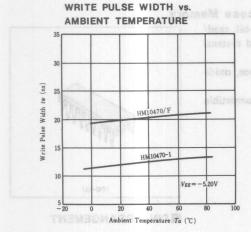
CHIP SELECT ACCESS TIME

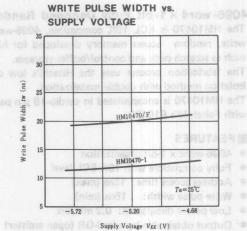


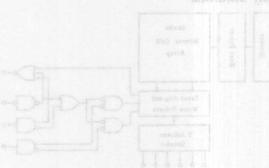
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE











HM10470-15

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.

FEATURES

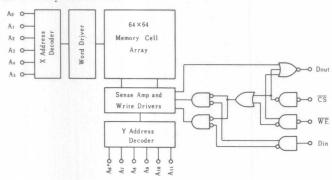
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 15ns (max)
 Write pulse width: 15ns (min)
- Low power dissipation: 0.2 mW/bit
- Output obtainable by wired-OR (open emitter)

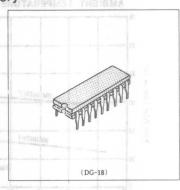
TRUTH TABLE

Input			Outrest	Mode	
CS	WE	Din	Output	Mode	
Н	×	×	L	Not Selected	
L	L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout *	Read	

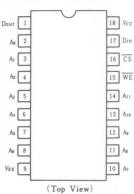
Notes) × : Irrelevant * : Read Out Nonivert

BLOCK DIAGRAM





PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	V_{in}	$+0.5$ to $V_{\it EE}$	V
Output Current	Iout	-30	mA
Storage Temperature	T_{stg}	-65 to $+150$	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-5.2$ V, $R_L=50\Omega$ to -2.0V, $T_a=0$ to +75°C, air flow exceeding 2m/sec)

un	Item	-	Symbol	Test Condition		min (B)	typ	max(A)	Unit
26			- 1		0°C	-1000		-840	n a nodmen
			V_{OH}		+25°C	-960	-	-810	
					+75°C	-900	<u> </u>	-720	
Output V	oltage	911	nise .	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1870	-	-1665	mV
		- 8	Vol		+25°C	-1850		-1650	Lupert Capi
		1			+75°C	-1830	-	-1625	Outgot Ca
			FIRM		0°C	-1020		-	
			Vonc		+25°C	-980	MA TI	DUNIE	TEST
				2. INPUT PULS	+75°C	-920	MD.	NONO2-8	mV
Output T	hreshold Vo	ltage		$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	_	1 8 -1	-1645	
			Volc		+25°C	-	1041	-1630	
				+75°C	_	-	-1605		
	(comment)		13/14/3	15 may 1	0°C	-1145		-840	
			VIH	Guaranteed Input Voltage High for All Inputs	+25°C	-1105	740U	-810	
				High for All Inputs	+75°C	-1045	1 -	-720	
Input Vol	itage				0°C	-1870	* +	-1490	mV
			V_{IL}	Guaranteed Input Voltage Low for All Inputs	+25°C	-1850	-	-1475	
				Low for All Inputs	+75°C	-1830	V0.5-	-1450	THE WALL
Іін		IIH	$V_{IN} = V_{IHA}$	0 to +75°C	-		220	14	
nput Current		CS	0 to +75°C	0.5	-	170	μΑ		
			IIL	Other $V_{IN} = V_{ILB}$	0 to +75 C	-50		2/101	
S l C.			7	All Input and Output Open,	Ta = 0 °C	-200	-160	-	- uncon
Supply C	urrent	-	I_{EE}	Test Pin 12	<i>Ta</i> = 75 °C		-145	/=	mA

ullet AC CHARACTERISTICS ($V_{\it EE} = -5.2\,{ m V} \pm 5\,\%$, Ta = 0 to $+75\,{}^{\circ}{ m C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs		-	-	8	ns
Chip Select Recovery Time	trcs		-		8	ns
Address Access Time	taa				15	ns

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	twsa=3ns	15			ns
Data Setup Time	twsp	*	2	-	_	ns
Data Hold Time	t_{WHD}	Parameter and the second	2	-	-	ns
Address Setup Time	twsA	t _W =15ns	3	-	_	ns
Address Hold Time	t_{WHA}	har was a found on	2	-	-	ns
Chip Select Setup Time	twscs	2 /ml	2			ns
Chip Select Hold Time	twHCS		2	_	-	ns
Write Disable Time	tws		_	-	8	ns
Write Recovery Time	t_{WR}	harman harman	_	-	8	ns

3. RISE/FALL TIME

Item	Symbol	0 0=5	Test Condition	.a - min) 8	typ	max	Unit
Output Rise Time	t.		Test Condition	Symbol	2	Tions	ns
Output Fall Time	t _f	T'a		-	2		ns
4. CAPACITANCE				Vase			
4. CAPACITANCE	100 C	17/20-4					
Item	Symbol	rea.	Test Condition	min	typ	max	Unit

TEST CIRCUIT AND WAVEFORMS

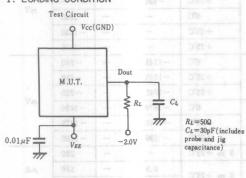
Cin

Cout

1. LOADING CONDITION

Input Capacitance

Output Capacitance



2. INPUT PULSE



_

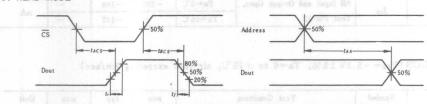
3

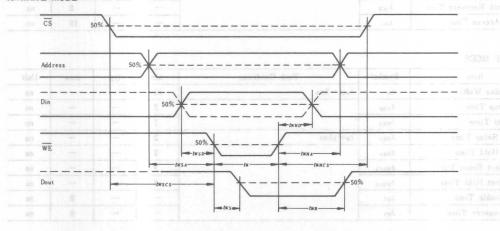
5

pF

pF

3. READ MODE





HM2142

4096-words × 1-bit Very High Speed Random Access Memory MANAGE ATTILIDED ATT

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM2142 is encapsulated in cerdip-20 pin package.

FEATURES

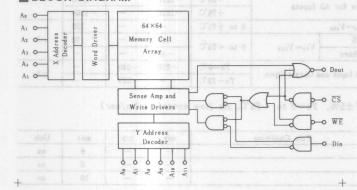
- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

TRUTH TABLE

Input			Outrout	Mode	
CS	WE	Din	Output	Mode	
Н	×	×	L	Not Selected	
L	Stat L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout *	Read	

Notes) ×: Irrelevant
*: Read Out Nonivert

BLOCK DIAGRAM





PIN ARRANGEMENT



O AC CHARACTERISTICS (Var-

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C) observe been a serve with year abrow-8904

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	$+0.5$ to V_{EE}	ALL SOUND A LINE
Output Current	Iout	-30	mA
Storage Temperature	Tate	-65 to +150	oold uprassCart
Storage Temperature	Tets (Bias)*	-55 to +125	JAN DOUTBULGIOUS

^{*} Under Bias

ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-5.2\text{V},~R_L=50\,\Omega$ to $-2.0\text{V},~T_d=0$ to $+75\,^{\circ}\text{C}$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
		I ING	0°C	-1000	0	-840	
	V_{OH}		+25°C	-980	65 (C. F)	-810	Write
			+75°C	-950	T-12-17-128	-720	18VVO S
Output Voltage		$V_{IH} = V_{IHA}$ or V_{ILB}	0°C	-1870	M. AU 310	-1665	mV
ANGEMENT	VOL		+25°C	-1850	-	-1650	TURT
			+75°C	-1830	-	-1625	
KOON (95)	1 34	Mode	0°C	-1020			
	V _{OHC}		+25°C	-980	180	21.VV	8.0
254 [41]		1 Scherred	+75°C	-920	× -	х	R
Output Threshold Voltage	3 7 7 7	$V_{IH} = V_{IHB}$ or V_{ILA}	0°C	_	1 -	-1645	mV
25 (1)	Volc	"I" spir	+25°C	-		-1630	
		(34)	+75°C		-	-1605	-
		500	0°C	-1165		-880	- 4
	V _{IH}	Guaranteed Input Voltage	+25°C	-1165	_	-880	La test
	e ;	High for All Inputs	+75°C	-1165	_	-880	
Input Voltage			0°C	-1810	_	-1560	mV
* =	V _{IL}	Guaranteed Input Voltage	+25°C	-1810	14.40	-1560	Divide a
		Low for All Inputs	+75°C	-1810	-	-1560	-0
4. 113	IIH	$V_{IN} = V_{IHA}$	0 to +75°C	-40	18 -	220	
put Current CS		CS	1.570	0.5	noscyni —	170	μA
	I_{IL}	Others $V_{IN} = V_{ILB}$	0 to +75°C	-50	Α	1 5 4 2	E
		10 1 20 0 0 0 To	Ta = 0°C	-270	-240	8 1	H -0 -
Supply Current	I_{EE}	All Input and Output Open.	Ta=75°C	-	-220	1	mA.

• AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, Ta = 0 to +75 °C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs		TEI		6	ns
Chip Select Recovery Time	trcs		0 0 0	0_0	6	ns
Address Access Time	taa	4	3 <u>5</u>		10	ns

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	$t_{WSA} = 3 \text{ns}$	10	_	_	ns
Data Setup Time	twsp		1	_	_	ns
Data Hold Time	t_{WHD}		1	_	_	ns
Address Setup Time	twsA	tw=10ns	3	_	_	ns
Address Hold Time	twhA		2	_	_	ns
Chip Select Setup Time	twscs		1	_	_	ns
Chip Select Hold Time	twncs		1	_	_	ns
Write Disable Time	tws		_	_	6	ns
Write Recovery Time	twn		_	_	6	ns

3. RISE/FALL TIME

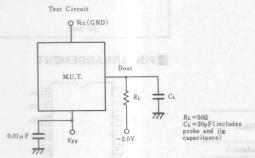
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t,	sublo, 1024-words x 4-pit rend	ame o xi0	2	i b#AOI	ns
Output Fall Time	t _f	oped for high speed systems such	ava b vio	2	ga mobr	ns ns

4. CAPACITANCE

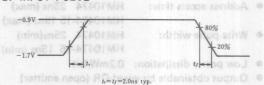
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	abligation parkets pinklinibas	ni bets	3	10474 is	pF
Output Capacitance	Cout		_	5	R al midor	pF

TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

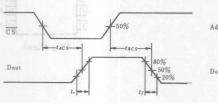


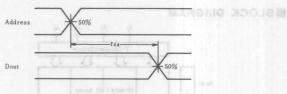
2. INPUT PULSE

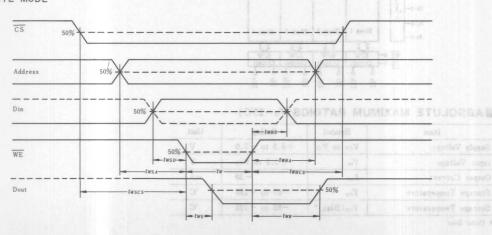


Fully compatible with 10K EQL

3. READ MODE







HM10474, HM10474-15

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time:

HM10474 25ns (max)

HM10474-15 15ns (max)

Write pulse width:

HM10474 25ns(min) HM10474-15 15ns (min)

• Low power dissipation: 0.2mW/bit

Output obtainable by wired-OR (open emitter)

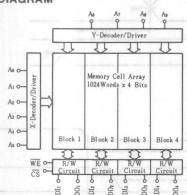
TRUTH TABLE

	Input	0	Made		
CS	WE	Din	Output	Mode	
Н	×	×	L	Not Selected	
L	L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout*	Read	

Notes) × : Irrelevant

* : Read Out Nonivert

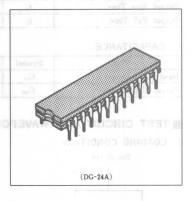
BLOCK DIAGRAM



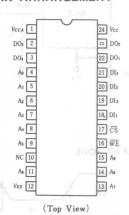
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to VEE	V
Output Current	Iout	-30	mA
Storage Temperature	Tets	-65 to +150	°C
Storage Temperature	Tota (Bias)*	-55 to +125	°C

* Under Bias



PIN ARRANGEMENT



ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-5.2$ V, $R_L=50\Omega$ to -2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
2			0°C	-1000		-840	al-glass
	Von		+25°C	-960	-	-810	
			+75°C	-900	- 1	-720	CAPAL
Output Voltage	die [$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1870	_	-1665	mV
74 - 1 1	Vol		+25°C	-1850	_	-1650	
90 - 57			+75°C	-1830		-1625	
	THE RE		0°C	-1020	_	_	
	Vonc		+25°C	-980	MA II	IOH12	
		2. INPUT PULSE	+75°C	-920	1401	10H03-04	I, LOAD
Output Threshold Voltage		$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	_	-	-1645	mV
1500 -X	Volc	†	+25°C	-	(043)	-1630	
			+75°C	-	-	-1605	
may 1	MARK	1 1	0°C	∸1145		-840	
	V_{IH}	Guaranteed Input Voltage	+25°C	-1105	rood -	-810	
and the same		High for All Inputs	+75°C	-1045		-720	
nput Voltage	1		0°C	-1870	5	-1490	mV
	VIL	Guaranteed Input Voltage	+25°C	-1850	-	-1475	
		Low for All Inputs	+75°C	-1830	9 _	-1450	
	IIH	$V_{IN} = V_{IHA}$	0 to +75°C	=:0 -	-	220	rice .
input Current	Take 1	CS		0.5		170	μΑ
	IIL	$V_{IN} = V_{ILB}$ Others	0 to +75°C	-50	-	_	
	HE	All Input and Output Open,	<i>Ta</i> = 0°C	-200	-160	30 <u>0</u> M	READ
Supply Current	IEE	Test Pin 12	Ta = 75°C	-	-145	/	mA

•AC CHARACTERISTICS ($V_{EE} = -5.2 \text{V} \pm 5\%$, Ta = 0 to $\pm 75^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

T. second	6 11	The Control	HM10474			HM10474-15			Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs		-	-	10		-	8	ns
Chip Select Recovery Time	t RCS		-	-	10	-	-	8	ns
Address Access Time	tAA		-	15	25	-	1	15	ns

Item	C	Test Condition		HM10474	1	ente H	M10474-	15	Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t _w	$t_{WSA} = 3$ ns	25	15	K11/	15		san	ns
Data Setup Time	t wsp	A***	2	_	A (2000)	2	-	<u>a10</u>	ns
Data Hold Time	t who	L. Miller	2	-	-	2	-	-	ns
Address Setup Time	t wsa	tw=twmin	3	1/-	1-	3	-	-	ns
Address Hold Time	t WHA	No.	2	ne neer	w	2		7	ns
Chip Select Setup Time	t wscs	MAT	2			2	1=1	_	ns
Chip Select Hold Time	t whees	30	2	-	-	2	1-	-	ns
Write Disable Time	t ws		11-	-	10		- 5-	8	ns
Write Recovery Time	ż _{WR}		100	-	10	-	_	8	ns

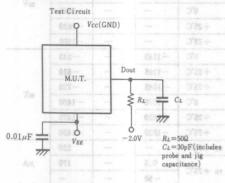
3. RISE/FALL TIME

(man Item and a	Symbol	Test Condition A VS.d-	min 3	typ	max	Unit
Output Rise Time	(e)t.	Test Caedition	Symbol	2	(0.04)	ns
Output Fall Time	neiti	0.6	_	2	-	ns
ots-						
1. CAPACITANCE						

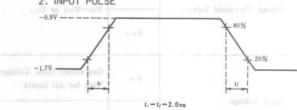
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cia	+25°C	409	4	_	pF
Output Capacitance	Cont	0.94.+	_	7	_	pF

TEST CIRCUIT AND WAVEFORMS



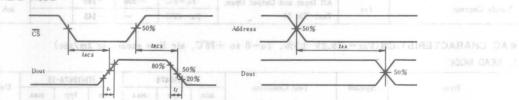


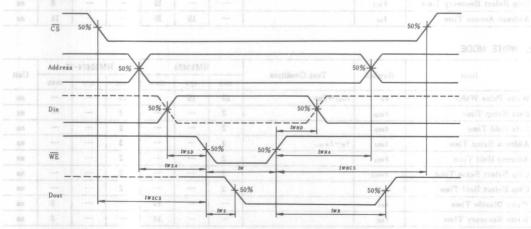
2. INPUT PULSE



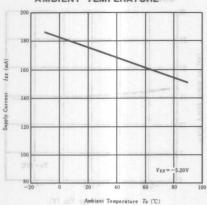
聚 ELECTRICAL CHARACTERISTICS

3. READ MODE

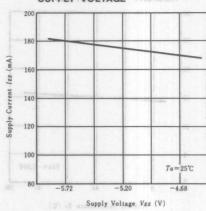




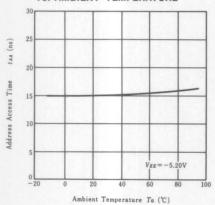
SUPPLY CURRENT vs.



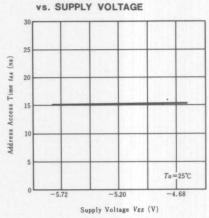
SUPPLY CURRENT vs. SUPPLY VOLTAGE



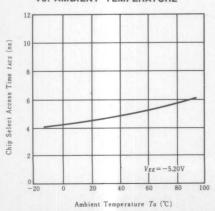
ADDRESS ACCESS TIME
vs. AMBIENT TEMPERATURE



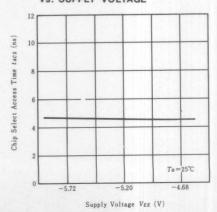
ADDRESS ACCESS TIME



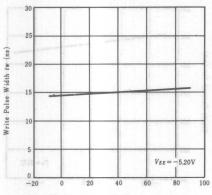
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



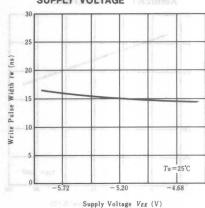
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs.

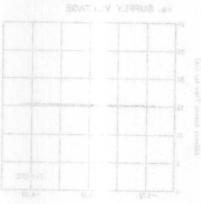


WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

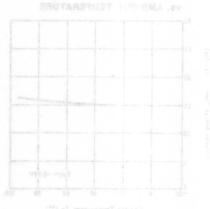


Ambient Temperature Ta (*C)

ADDRESS ACCUSS TIME



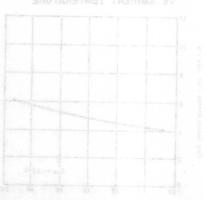
ADDRESS ACCESS TIME



CHIP SELECT ACCESS TIME



CHUP SELECT ACCESS TIME



HM10480, HM10480F

16,384-words × 1-bit Fully Decoded Random Access Memory

The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

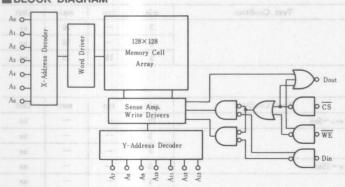
TRUTH TABLE

Input			0	Mode
CS	WE	Din	Output	Mode
Н	×	×	grant L	Not Selected
L	L	L	L	Write "0"
L	L 041	Н	L	Write "1"
L	H OSI-	×	Dout*	Read

Notes) × : Irrelevant

* : Read Out Noninvert

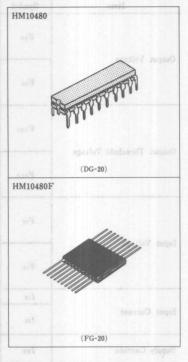
■BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to VCC	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to V _{EE}	V
Output Current	Iout	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	Tstg(Bias)*	-55 to +125	°C

^{*} Uniter Bias



PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS ($V_{EE}=-5.2$ V, $R_L=50\Omega$ to -2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
	081E.151B	for high speed	anclave 0°C	-1000	acces	-840	tirw/bss
	Von	storages,	+25°C	-960	isiq ri toli g	-810	g america
	100	$-V_{IN} = V_{IHA} \text{ or } V_{ILB}$	+75°C	-900	ru 28 55 0	-720	ndst pr
Output Voltage		- VIN = VIHA OF VILB	0°C	-1870	uob m iv	-1665	mV neizalo
A Property of the Control of the Con	Vol	niq-02 relt bns n	+25°C	-1850	brd st ra e	-1650	MH ed
197790000	1 1		+75°C	-1830	driv <u>u</u> sk	-1625	ac'sage,
11779			0°C	-1020	_	_	
	Vonc		+25°C	-980	-	_	
Output Threshold Voltage			+75°C	-920	_	_	1
		$V_{IN} = V_{IHB}$ or V_{ILA}	0°C		2-	-1645	mV
	Volc		+25°C	Masiria Ma Masiria Masiria Masiria Masiria Masiria Masiria Ma	0.110_1 2	-1630	16,00
	.08801686		+75°C	Leade	7131 VI QU	-1605	VHIII-)
			0°C	-1145	- Total	-840	mV
	VIH	Guaranteed Input Voltage	+25°C	-1105	enoi si Lia	-810	
din		High for All Inputs	+75°C	-1045	a vet a tele	-720	
Input Voltage			0°C	-1870	_	-1490	
	VIL	Guaranteed Input Voltage	+25°C	-1850	_	-1475	
	200	Low for All Inputs	+75°C	-1830		-1450	
	IIH	$V_{IN} = V_{IHA}$ sholf	0 to +75°C		100	220	88
Input Current		CS	0 1 5 7 7 7	0.5	-	170	μΑ
	IIL	$V_{IN} = V_{ILB}$ Others	0 to +75°C	-50	-		- 1
(02 CYT)		All Input and Output Open,	Ta = 0°C	-170	-140		J.
Supply Current	IEE	Test Pin 10	Ta = 75°C	×-	-130	-	mA

•AC CHARACTERISTICS ($V_{EE} = -5.2 \text{V} \pm 5\%$, Ta = 0 to $+75^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

	Itam Sumbal Tast Condition			14-1-41	77.1			
Item	Symbol	Test Condition	min	typ	max	Unit		
Chip Select Access Time	tacs		2		10	ns		
Chip Select Recovery Time	trcs		2 × 852	-	10	ns		
Address Access Time	taa		3	15	25	ns		

Symbol	Test	Condition	min	typ	max	Unit
t w	$t_{WSA} = 5$ ns		25	19	_	ns
twsp	awa po	13) [5	-	-	ns
t who			5	-	-	ns
twsa	tw = 25 ns	. 66	6 5 6	9 7	_	ns
t wha		5 5	5	5- <u>+</u>	-	ns
twscs			5	_	_	ns
twncs		\$ (Ta=20°C)	5	ME MADY	-5	ns
tws	Unit		odav y?	-	10	ns
twn	V		Vig-to Vie	_	10	ns
	tw twsd twhd twsa twha twscs twhcs tws	tw twsa=5ns twsD twhD twsA twsA tw=25ns twhA twscs twhcs tws	tw twsa=5ns twsD twhD twsA tw=25ns twhA twscs twhcs tws	tw twsa=5ns 25 twsD 5 twhD 5 twsa tw=25ns 5 twhA 5 twscs 5 twhcs 5 tws 5	tw twsa=5ns 25 — twsD 5 — twhD 5 — twsA tw=25ns 5 — twhA 5 — twscs 5 — twhcs 5 — tws 5 —	tw twsa=5ns 25 — twsd 5 — — twhd 5 — — twsa tw=25ns 5 — — twha 5 — — twscs 5 — — twhcs 5 — 5 tws — — 10

.... igyaJ e

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.	Udit, read-furite random access	x trow	2	1 8 17 00	ns
Output Fall Time	t,		oite o lige	2	develope	ns

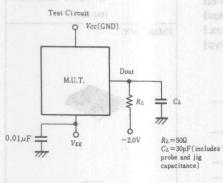
DUCTAUOTNIH, CTA

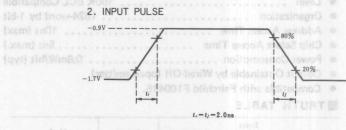
4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	ls ancapsulated in cerdip-16pin	yhor <u>m</u> ain	4	35.J75_9210	pF
Output Capacitance	Cont		-	7	-	pF

TEST CIRCUIT AND WAVEFORMS

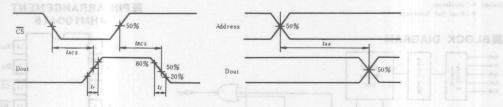
1. LOADING CONDITION

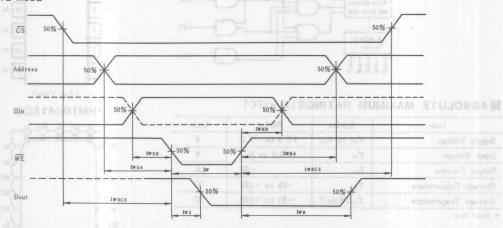




buffer storages which require very high speeds.

3. READ MODE





HM100415,HM100415CC

1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

FEATURES

- Chip Select Access Time 5ns (max.)
- Power Consumption 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

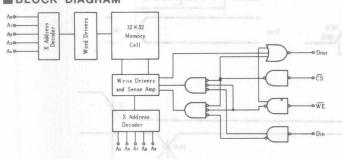
TRUTH TABLE

	Input	0	Mode	
CS	WE	Din	Output	
Н	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L,	Н	L	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant

* : Read Out Noninvert

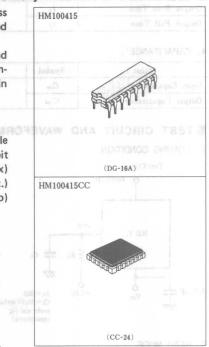
BLOCK DIAGRAM



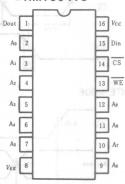
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to VEE	V
Output Current	Iout	-30	mA
Storage Temperature	Tets	-65 to +150	°C
Storage Temperature	Tota (Bias)*	-55 to +125	°C

* Under Bias

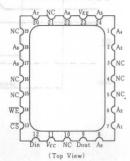


■ PIN ARRANGEMENT ● HM100415



(Top View)

●HM100415CC



■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-4.5$ V, $R_L=50\Omega$ to -2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Ven T	est Condition	min(B)	typ	max(A)	Unit
/	Von	Vis - VIHA OF VILB		-1025	-955	○-880	mV
Output Voltage	Vol			-1810	-1715	-1620	mV
O	Vonc	V = V · · · · · · · · · · · · · · · · ·		-1035		-	mV
Output Threshold Voltage	Volc	$V_{in} = V_{IHB}$ or V	ILA			-1610	mV
Input Voltage	VIH	Guaranteed Input Voltage High/Low for All Inputs		-1165	-	-880	mV
	VIL			-1810	- 1	-1475	mV
	IIH	$V_{in} = V_{IHA}$		b	-	220	μΑ
Input Current			CS autoliani Fight =	0.5	-	170	μA
	IIL	$V_{in} = V_{ILB}$	Others	-50	-	-	
Supply Current	IEE	All Inputs and Outputs Open		-200	-150	-	mA

•AC CHARACTERISTICS ($V_{EE} = -4.5 \text{V} \pm 5\%$, Ta = 0 to $\pm 85^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs	200 Date	-	3	5	ns
Chip Select Recovery Time	trcs		_	3	5	ns
Address Access Time	taa		-	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 2$ ns	6	4		ns
Data Setup Time	t ws D	*	2	0	- New York	ns
Data Hold Time	t who		2	0		ns
Address Setup Time	twsa	tw=6ns	2	0	- 4	ns
Address Hold Time	t wha		2	0		ns
Chip Select Setup Time	twscs		2	0		ns
Chip Select Hold Time	twhcs	A Second	2	0	_ 70	ns
Write Disable Time	tws	(300)		3	5	ns
Write Recovery Time	t wr	4	riem-	3	5	ns

3. RISE/FALL TIME

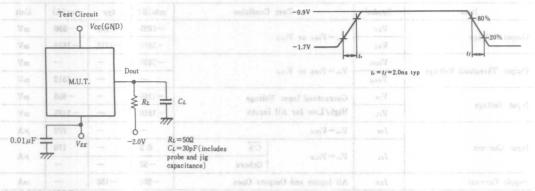
Item	Symbol	Test Condition	min	typ	máx	Unit
Output Rise Time	t.		-	2	-	ns
Output Fall Time	t _f		-	2	-	ns

4. CAPACITANCE

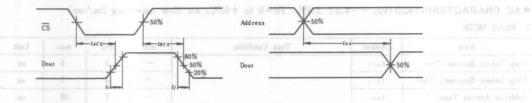
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin		-	3	_	pF
Output Capacitance	Cout		-	5	-	pF

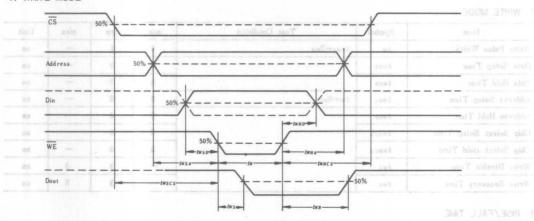
TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION IN THE START OF START OF START PULSE 12 1831 START OF START OF



3. READ MODE





	Xám		Test Condition		Item
80					
				1,1	

.tinEl	199	Yest Condition	Joseph	
Fig				Output Cameritance

HM100422,HM100422F HM100422CC

256-word×4-bit Fully Decoded Random Access Memory

The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

FEATURES

- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

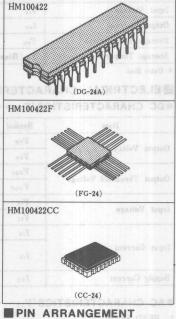
TRUTH TABLE

	Input	0.00000		
BS	WE	Din	Output	Mode
Н	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	ne H	×	Dout*	Read

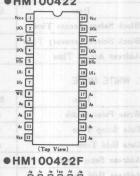
Notes) × : Irrelevant

* : Read Out Noninvert

BLOCK DIAGRAM Y-Decoder/Driver Ao O-Memory Cell Array 256 Words ×4 Bits A1 0-A2 0-A3 0 Ai O Block 3 Block 4 R/W Circuit R/W Circuit R/W Circuit R/W Circuit 9 9 9 9 9 9 BESI DOI DIS DIS BS3 UIs DOS BS, UI,

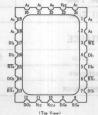


●HM100422



Uls [DI. C BS, BSt

●HM100422CC



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
nput Voltage	Vin	$+0.5$ to V_{EE}	movne
Output Current	Iout	30	mA
Storage Temperature	Tota	-65 to $+150$.c
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

^{*} Under Bias

■ ELECTRICAL CHARACTERISTICS NO consider work a liberial and a carpon contained and

•DC CHARACTERISTICS ($V_{EE} = -4.5\text{V}$, $R_L = 50\Omega$ to -2.0V, $T_a = 0$ to $+85^{\circ}\text{C}$, air flow exceeding 2m/sec)

Item	Symbol	T 24pm	est Condition	min(B)	typ	max(A)	Unit
	Von		d's F100422.	-1025	-955	-880	mV
Output Voltage	Vol	$-V_{in}=V_{IHA} \text{ or } V$	ILB	-1810	-1715	-1620	mV
0	Vонс	$V_{in} = V_{IHB}$ or V_{in}		-1035	sineg ro I	id-A x -b s	mV
Output Threshold Voltage	Volc	Vin = VIHB or V	ILA laval	OH ECL	is ani u i	-1610	mV
	VIH	Guaranteed Inpu	ut Voltage	-1165	mit i i (m	-880	mV
Input Voltage	VIL	High/Low for	All Inputs	-1810	blw saluc	-1475	mV
	Іін	$V_{in} = V_{IHA}$	1	44/4/1 <u>m</u> 2)	partion: (220	μΑ
Input Current			BS (restrime nace	0.5	aw Agrae	170	rughuU
	IIL	$V_{in} = V_{ILB}$	Others	-50	_	_	μΑ
Supply Current	IEE	All Inputs and	Outputs Open	-200	-165	JOAL 1	mA

• AC CHARACTERISTICS ($V_{EE} = -4.5 \text{V} \pm 5\%$, Ta = 0 to $+85^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	tabs	0 51035			5	ns
Block Select Recovery Time	trbs		- 22		5	ns
Address Access Time	taa	Dout" Read	×	7	10	ns

2. WRITE MODE

Item	Symbol		Test Con	dition	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 2$ ns	-		6	4.5	_	ns
Data Setup Time	twsp			-Decoder/Detect	2	0	_	ns
Data Hold Time	t wh D				2	0	-	ns
Address Setup Time	twsA	tw = 6ns			2	0	_	ns
Address Hold Time	t wha		-		2	0	_	ns
Block Select Setup Time	twsss				2	0	-0 M	ns
Block Select Hold Time	twhbs			Memory Coll Array	2	0	-	ns
Write Disable Time	tws			- tog extend to	-	4	5	ns
Write Recovery Time	twr				_	4.5	9	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.		-	2	-C-10	ns
Output Fall Time	. t _f	2 Block C Block a	lan 8	2	-	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	The state of the s		4	-	pF
Output Capacitance	Cout		0 0 1	7	-	pF

TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION wromen associa mr. 2. INPUT PULSE of white did-1 x brow- 300 A Test Circuit 10 11 10 Very Vandom access O Vcc(GND) tems such as scratch pads and process is the Hideo isolation method with double metalic Dout M.U.T. The HATTODAYO & comparible with the HOTODIX ECL families and $t_t - t_f - 2.0$ ns typ $\leq R_L$ proyed noise margin. This device is encapsulated in cerdin-18pin 9 0.01µF = -2.0V $R_L = 50Q$ $C_L = 30 p F (includes)$ m probe and jig capacitance) 3. READ MODE (Seat(max) 50% Address tras - tans anistrio funtion Dout 4. WRITE MODE BS 50% Address 聞きLOCK DIAGR Din WE -0 4 Dout

	Indured	
		Supply Voltage
	Tine .	
	Ter (Bias)*	

HM100470,HM100470-15

25ns(max)

4096-word×1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.

FEATURES

- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: HM100470
- HM100470-15 15ns(max)
- Write pulse width: HM100470 25ns (min)
 - HM100470-15 15ns (min)

Output obtainable by wired-OR (open emitter)

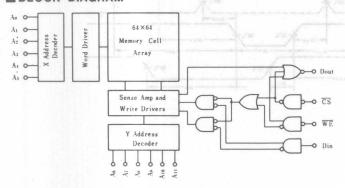
TRUTH TABLE

	-	Input	0	No.	
	CS	WE	Din	Output	Mode
	Н	×	×	L	Not Selected
	L	L	L	L	Write "0"
	L	L	Н	L	Write "1"
-	L	Н	×	Dout*	Read

Notes) × : Irrelevant

* : Read Out Nonivert

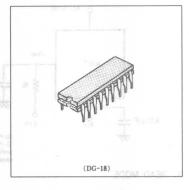
BLOCK DIAGRAM



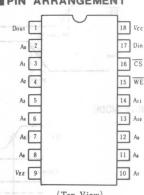
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to VEE	V
Output Current	Iout	-30	mA
Storage Temperature	Talg	-65 to +150	°C
Storage Temperature	Tata (Bias)*	-55 to +125	°C

^{*} Under Bias



PIN ARRANGEMENT



(Top View)



BITEST CIRCUIT AND WAVEFORMS

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-4.5$ V, $R_L=50\Omega$ to -2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Tex.T	est Condition	min(B)	typ	max(A)	Unit
	Von			-1025	-955	-880	mV
Output Voltage	Vol	$V_{in} = V_{IHA}$ or V	ILB	-1810	-1715	-1620	mV
parent .	Vонс	140		-1035	-1	-	mV
Output Threshold Voltage	Volc	$V_{in} = V_{IHB}$ or V	ILA	1 -	- ASILM	-1610	mV
	VIH	Guaranteed Inp	Guaranteed Input Voltage		-	-880	mV
Input Voltage	VIL	High/Low for	-1810	TL-	-1475	mV	
	IIH	$V_{in} = V_{IHA}$	Date of	V 3	0 -	220	μA
Input Current			CS	0.5	_	170	
	IIL	$V_{in} = V_{ILB}$ Others		-50	-	-	μA
Supply Current	IEE	All Inputs and	All Inputs and Outputs Open		-165	90000	mA

•AC CHARACTERISTICS ($V_{EE} = -4.5 \text{V} \pm 5\%$, Ta = 0 to $+85^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

			148 - 230 - 464 [187 - 234] 1774						
Item	Symbol Test Condition		HM100470-15			HM100470			Unit
		min	typ	max	min	typ	max	Onit	
Chip Select Access Time	tacs		-	-	8	- 100	-	10	ns
Chip Select Recovery Time	trcs		-	_	8	-	-	10	ns
Address Access Time	t AA		-	-	15	-	J	25	ns

2. WRITE MODE

Item	C-1-1	T C 1:-:	Н	M100470-	-15	HM100470			Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 3$ ns	15	_		25	-	-	ns
Data Setup Time	twsp	H	2	-	VE	2	-		ns
Data Hold Time	t who		2		1	2	-		ns
Address Setup Time	twsa	tw=twmin	3	7		3		-	ns
Address Hold Time	t wha	1	2	1200	l -	2	-	- <u>2</u> w	ns
Chip Select Setup Time	twscs	2 35/0 12-12	2	- T	1487 - 00	2	-	-	ns
Chip Select Hold Time	t whes		2	radiment on		2	-	Dour	ns
Write Disable Time	t ws	1	-	-	8	-	-	10	ns
Write Recovery Time	t wR		_ Peaco	-	8	-	-	10	ns

3. RISE/FALL TIME

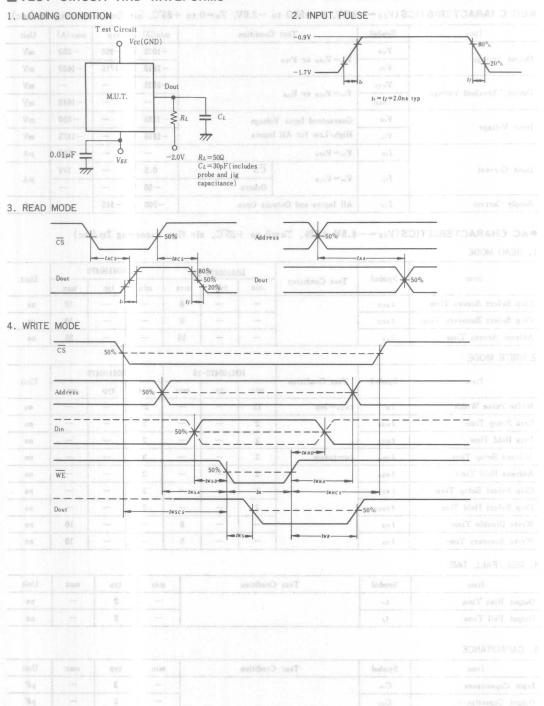
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.		-	2	-	ns
Output Fall Time	t,		_	2		ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin		- 1	3	-	pF
Output Capacitance	Cout		_	5	-	pF

TEST CIRCUIT AND WAVEFORMS

BELECTRICAL CHARACTERISTICS



HM100474,HM100474-15 HM100474F,HM100474F-15

1024-word×4-bit Fullý Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

FEATURES

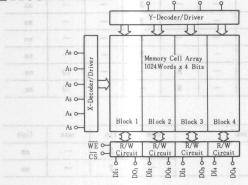
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474/F 25ns(max)
 - HM100474/F-15 15ns(max)
- Write pulse width: HM100474/F 25ns(min) HM100474/F-15 15ns(min)
- Output obtainble by wired-OR (open emitter)

TRUTH TABLE

	Input		0.44	Mode
CS	WE	Din	Output	Mode
Н	×	×	L	Not Selected
L	L) 75001	AL L	8x-7 L 171091	Write "0"
L	nam L qui	Н	typ L gyr	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

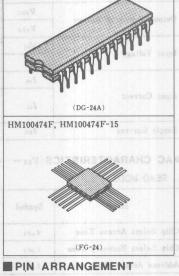
BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to VEE	V
Output Current	Iout	-30	mA
Storage Temperature	Tate	-65 to +150	°C
Storage Temperature	Tate (Bias)*	-55 to +125	°C

^{*} Under Bias

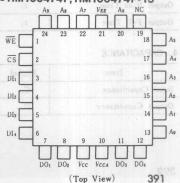


HM100474, HM100474-15

●HM100474.HM100474-15



●HM100474F, HM100474F-15



■ ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS ($V_{EE}=-4.5\mathrm{V},~R_L=50\Omega$ to $-2.0\mathrm{V},~Ta=0$ to $+85^{\circ}\mathrm{C},~air$ flow exceeding 2m/sec)

Item	Symbol	res Memer	est Condition	min(B)	typ	max(A)	Unit
	Von		4-bit, read/write, tand	-1025	-955	-880	mV
Output Voltage	Vol	$V_{in} = V_{IHA}$ or V	ILB grow are remained armadely	-1810	- 1715	-1620	mV
1 doi:10 l	Voнc		mehic low considera-	-1035	i azanaa	g notica	mV
Output Threshold Voltage	Volc	$V_{in} = V_{IHB}$ or V		itaram ol	duab Thi	-1610	mV
TANKS S. S. S. S.	VIH	Guaranteed Inp	111000000000000000000000000000000000000		dedeo	-880	mV
Input Voltage	VIL	High/Low for	-1810	, eph <u>Ho</u> v	-1475	mV	
	IIH	$V_{in} = V_{IHA}$	copsulated in cerdip-24	ula si cipiline	@ 59. (_1)	220	μΑ
Input Current			CS	0.5	13 Prilitary	170	
III.		$V_{in} = V_{ILB}$	$V_{ia} = V_{ILB}$ Others		_	838	μΑ
Supply Current	IEE	All Inputs and	All Inputs and Outputs Open		-165	- x <u>m</u> o	mA

•AC CHARACTERISTICS ($V_{EE}=-4.5\mathrm{V}~\pm5\%$, Ta=0 to $+85^{\circ}\mathrm{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol Test Condition -	m . G . 1:::	HM100474/F-15			HM100474/F			Unit
		min	typ	max	min	typ	max	Unit	
Chip Select Access Time	tacs		-	-	8	_	-9	10	ns
Chip Select Recovery Time	trcs		-	-	8			10	ns
Address Access Time	taa 9	abo	16	<u>1</u> (1910	15	nid.	15	25	ns

2. WRITE MODEO PARM, ANT LOTHING to be belief a bull to a later of the later of the

10 (10)	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
Item	Symbol Test Condition	lest Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 3$ ns	15	the	-	25	15		ns
Data Setup Time	t ws D		2	-	T -	2		Juans Charle None	ns
Data Hold Time	t who		2	-	_	2	14.67	45 A 179	ns
Address Setup Time	t ws A	t w=twmin	3	-	9 -9	9 3	101.141.1	DATE:	ns
Address Hold Time	t wha		2		osbe <u>r/</u> Driver	2		-	ns
Chip Select Setup Time	twics		2	-32	1	2	1-1	-	ns
Chip Select Hold Time	t whcs		2	-	Sent Tio	2		c 4 <u>c</u>	ns
Write Disable Time	t ws		_	-	8	4/1201	- 10	10	ns
Write Recovery Time	t wr	1	-	-	8	+	1-18	10	ns

3. RISE/FALL TIME

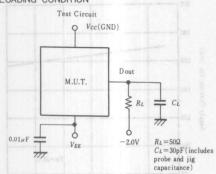
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.	West & William Controls	WVE Tuenta	2	_	ns
Output Fall Time	t,		8 -	2	-	ns

4. CAPACITANCE

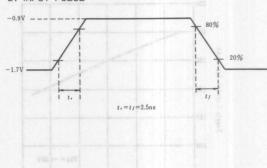
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	V 0.0- 01 0.0-	10/4 /03 3/1/4	4	- 78	pF
Output Capacitance	Cout		_	7		pF

TEST CIRCUIT AND WAVEFORMS

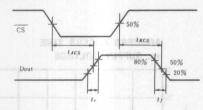
1. LOADING CONDITION

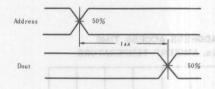


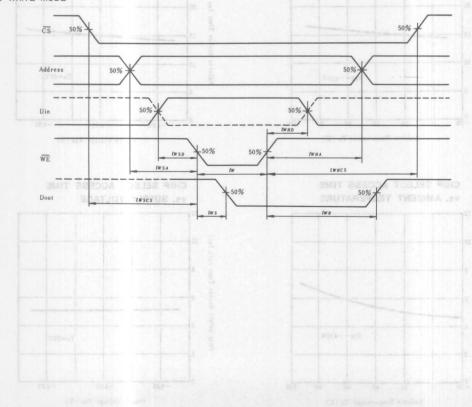
2. INPUT PULSE



3. READ MODE







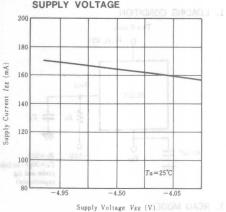
 $V_{EE} = -4.50 \text{V}$

AMBIENT TEMPERATURE 200 180 (Y# 160 140 ... 140 ... 120

100

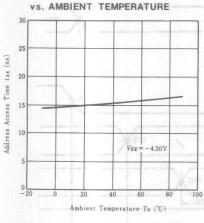
SUPPLY CURRENT vs.



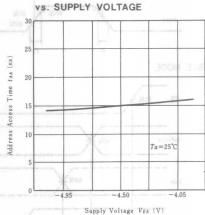


ADDRESS ACCESS TIME

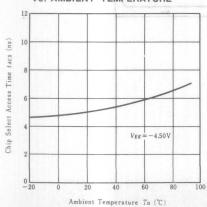
Ambient Temperature Ta (°C)



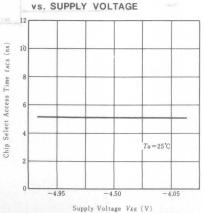
ADDRESS ACCESS TIME

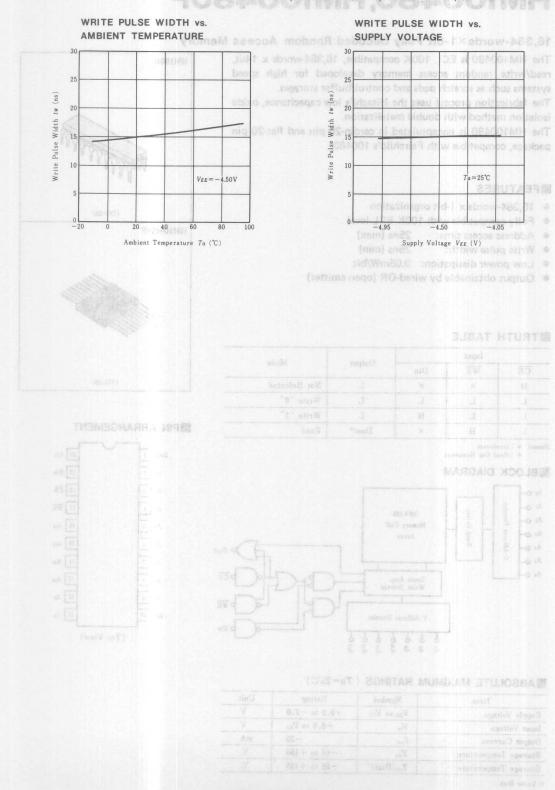


CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



CHIP SELECT ACCESS TIME





HM100480, HM100480F

16,384-words×1-bit Fully Decoded Random Access Memory

The HM100480 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100480 is encapsulated in cerdip-20 pin and flat-20 pin package, compatible with Fairchild's 100480.

FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time:

25ns (max)

Write pulse width:

25ns (min)

Low power dissipation: 0.05mW/bit

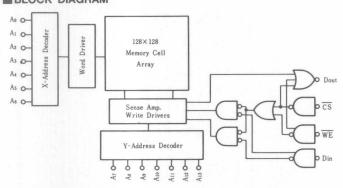
Output obtainable by wired-OR (open emitter)

TRUTH TABLE

	Input		0	Mode Not Selccted Write "0"
CS	WE	Din	Output	Mode
Н	×	×	L	Not Selccted
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

Notes) ×: irrelevant * : Read Out Noninvert

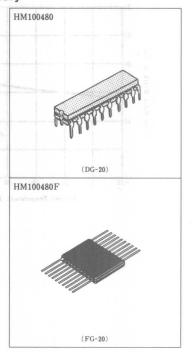
BLOCK DIAGRAM



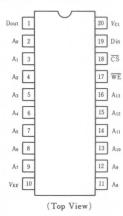
BABSOLUTE MAXIMUM RATINGS ($Ta=25^{\circ}C$)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vin	+0.5 to V _{EE}	V
Output Current	Iout	-30	mA
Storage Temperature	Tata	-65 to +150	°C
Storage Temperature	Tstg(Bias)*	-55 to +125	°C

* Under Bias



PIN ARRANGEMENT



MADSOLUTE MAXIMUM RATINGS $(Ta=25^{\circ}C)$

Item	Symbol	Rating	Unit
Supply Voltage	V _{EE} to V _{CC}	+0.5 to -7.0	V.
Input Voltage	·Vin	$+0.5$ to V_{EE}	V
Output Current	Iout	-30	mA
Storage Temperature	Tats	-65 to +150	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

^{*} Under Bias

ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{EE}=-4.5\text{V}$, $R_L=50\Omega$ to -2.0V, Ta=0 to $+85^{\circ}\text{C}$, air flow exceeding 2m/sec)

		THOUSE THEORET	C. C		18750	Bell & Arthur Strain	H13.175
Item	Symbol	T	Test Condition		typ	max(A)	Unit
Carl Carl	V_{OH}	¥		-1025	-955	-880	mV
Output Voltage	Vol	$V_{in} = V_{IHA}$ or V_{in}	ILB	-1810	-1715	-1620	mV
O The last Mark	V_{OHC}	V V V		-1035	-	-	mV
Output Threshold Voltage	Volc	$V_{in} = V_{IHB}$ or V	$V_{in} = V_{IHB}$ or V_{ILA}		50G - L	-1610	mV
T . 37 1.	V_{IH}	Guaranteed Inp	Guaranteed Input Voltage			-880	mV
Input Voltage	V_{IL}	High/Low for All Input		-1810	3 +	-1475	mV
	I_{IH}	$V_{in} = V_{IHA}$	Retrod@ Ce=NoFF collabor	1117	1 -	220	μΑ
Input Current		77 77	$V_{In} = V_{ILB}$ Others		10.8-	170	and State
	I_{IL}	$V_{in} = V_{ILB}$				-	μA
Supply Current	I_{EE}	All Inputs and	Outputs Open	-200	-165	_	mA

•AC CHARACTERISTICS ($V_{EE} = -4.5 \text{V} \pm 5\%$, Ta = 0 to $+85^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs	200	2	3/-	10	ns
Chip Select Recovery Time	tres		2	1 *	10	ns
Address Access Time	tAA		3	546-13	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t _w	$t_{WSA} = 5 \text{ns}$	25		16-	ns
Data Setup Time	twsp	¥	5	=	-	ns
Data Hold Time	t_{WHD}		5			ns
Address Setup Time	twsA	$t_W = t_W \min$	5			ns
Address Hold Time	t _{WHA}	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	5	-	_	ns
Chip Select Setup Time	twscs	(max m	5		_	ns
Chip Select Hold Time	twhcs	1000	-	-	5	ns
Write Disable Time	tws			1 -	10	ns
Write Recovery Time	t _{WR}	A	_	-	10	ns

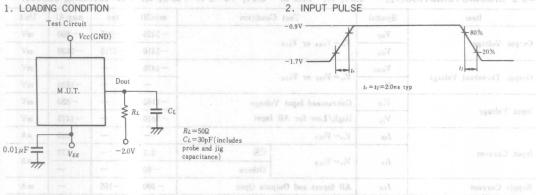
3. RISE/FALL TIME

Item	Symbol	siaU	Test Condition	ferlag	min	typ	max	Unit
Output Rise Time	t.	V	40.5 to -7.0	Total at a	N T	2	mest	ns
Output Fall Time	t _f	Age			No.	2	-	ns

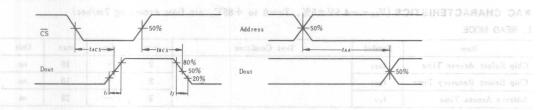
4. CAPACITANCE

Item	Symbol		Test Condition	-	min	typ	max	Unit
Input Capacitance	Cin	3	-55 to +125	"Tasid),		3	charl standard	pF
Output Capacitance	Cont				_	5	_	pF

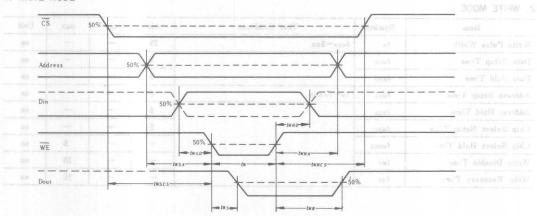
TEST CIRCUIT AND WAVEFORMS



3. READ MODE



4. WRITE MODE

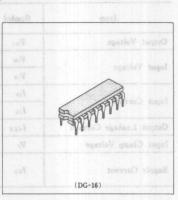


HM2504, HM2504-1

256-word×1-bit Fully Decoded Random Access Memory

The HM2504 Series item is a TTL compatible, 256-word x 1-bit, read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. This is a fully decoded, read/write random access memory perfectly compatible with the TTL logic family, designed as an open collector output type for simplicity of expansion.

- Level TTL compatible
- Construction 256-word x 1 bit
- - HM2504-1: 45ns (max.)
- Chip select access time 30ns (max.)
- Power consumption 1.8mW/bit (typ)
- Output Open collector



ODC CHARACTERISTICS (No.

PIN ARRANGEMENT

TR	UTH	TAB	LE
himbi	- 27.5	an .	rock .

		Inputs	M KEST	Output	
CS	60	WE	Din	Open Collector	Mode
any one	Н	×	×	8 Н	Not Selected
all	L	L	L	Н	Write "0"
all	L	L	Н	Н	Write "1"
all	L	Н	×	Dout*	Read

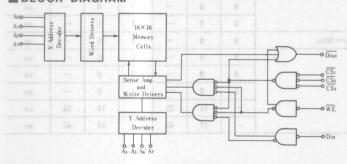
Notes) × : Don't care

* : Read out inverted

A₀ 1 16 V_{CC} A₁ 2 15 A₂ CS₁ 3 14 A₂ CS₂ 4 13 Din CS₃ 5 12 WE Dout 6 111 A₇ A₄ 7 10 A₆ GND 8 9 A₅

(Top View)

BLOCK DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item (1)	Symbol	HM2504, HM2504-1	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	Vin	-0.5 to +5.5	V
Input Current	Iin	-12 to +5.0	mA
Output Voltage (Output High)	Vout	-0.5 to +5.5	V
Output Voltage (DC Output Low)	Iout	+20	mA
Storage Temperature	$T_{st_{\mathcal{S}}}$	-65 to +150	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

^{*} Under Bias

■ ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS ($V_{cc}=5.0 \text{V} \pm 5\%$, $T_a=0$ to $+75^{\circ}\text{C}$, air flow exceeding 2 m/sec)

Y	C 1 -1	Jid-1 × Into	. compatible	HM2504 Series			Unit
Item	Symbol	Symbol Test Condition		min	typ	max	Unit
Output Voltage	Vol	Vcc=4.75V, IoL=	16mA - 19902-1011	ne m ories	0.3	0.45	V
	VIH	Guaranteed Input	Guaranteed Input Voltage High		1.6	INTER CER	V
Input Voltage	VIL	Guaranteed Input Voltage Low		mer bigo	1.5	0.85	V
	IIH	Vcc=5.25V, Vin=	4.5V	_	0	20	μA
Input Current	IIL	Vcc=5.25V, Vin=0			-530	-800	μA
Output Leakage Current	ICEX	Vcc=5.25V, Vout=	4.5V		0	50	μA
Input Clamp Voltage	V _I	Vcc=5.25V, Iin=	-10mA	_	-1.0	-1.5	V
		Vcc=5.25V	0< Ta < 25°C	<u></u>	3/11/1/ 201	135	mA
Supply Current	Icc	All input GND	<i>Ta</i> ≥25°C		_	130	mA

•AC CHARACTERISTICS

 $(V_{cc}=5.0V \pm 5\%, T_a=0 \text{ to } +75^{\circ}\text{C}, \text{ air flow exceeding } 2\text{m/s}, \text{ see test circuit and waveforms})$

1. READ MODE

A [8]			100	HM2504		1	HM2504-	RT HI	URT
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs	Node N	-	12	30	-	12	30	ns
Chip Select Recovery Time	trcs		-	18	25	-	18	25	ns
Address Access Time	taa		-	35	55	-	30	45	ns

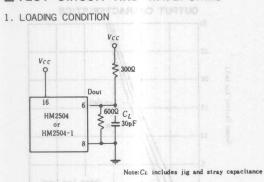
2. WRITE MODE

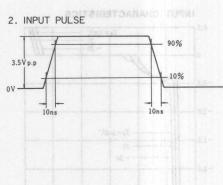
A () A	Chal	Test Condition		HM2504		1	HM2504-	1	Unit
Item	Symbol	lest Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	$t_{WSA} = 0_{ns}$	30	8	_	30	8	10 300	ns
Data Setup Time	twsp		0	0	-	0	0		ns
Data Hold Time	t wh D		5	0	-	5	0	1	ns
Address Setup Time	twsa	tw = 30 ns	0	0	-	0	0	7711	ns
Address Hold Time	t wha	ino-CE	5	0	1 -	5	0	1 -	ns
Chip Select Setup Time	twscs		0	0	1-	0	0	-	ns
Chip Select Hold Time	t whcs		5	0	100	5	0	_	ns
Write Disable Time	t ws	77()FL	11	14	35		14	35	ns
Write Recovery Time	t wr		_	12	40	MANAGE TO SERVICE TO S	12	40	ns

3. CAPACITANCE

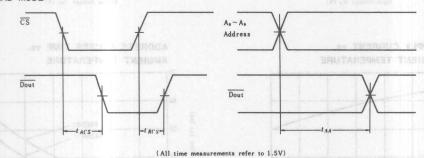
Item	Symbol	Test Condition			HM2504		HM2504-1		
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Input Capacitance	Cin		0	3	5	_	3	5	pF
Output Capacitance	Cout		0.0 -	6	8	_	6	8	pF

TEST CIRCUIT AND WAVEFORMS

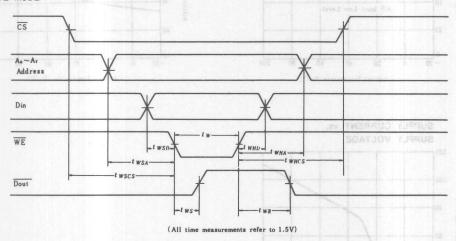


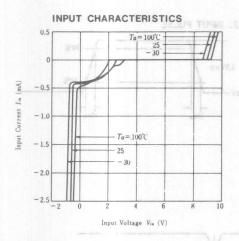


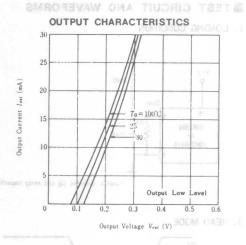
3. READ MODE

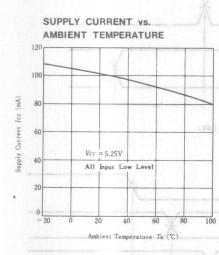


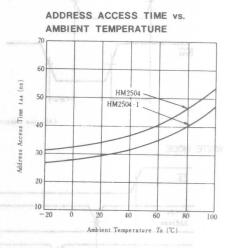
4. WRITE MODE

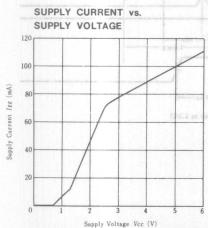












HM2510, HM2510-1, HM2510-2

1024-word × 1-bit Fully Decoded Random Access Memory
The HM2510 Series item is a 1024-word x 1-bit read/write random
access memory developed for application to buffer memories,
control memories, high-speed main memories, etc. It is a fully
decoded, read write, random access memory perfectly compatible
with TTL logic families, designed as an open collector output type

for simplicity of expansion.

• Level TTL compatible

Construction 1024-word x 1 bit

Read access time HM2510: 70ns (max.)

HM2510-1: 45ns (max)

HM2510-2: 35ns (max.)

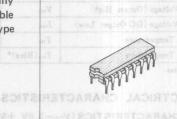
Chip select access time HM2510: 40ns (max.)

HM2510-1: 30ns (max.)

HM2510-2: 25ns (max.)

Power consumption 0.5mW/bit

Output Open collector



WALLSOLUTE HAXIMUM RATINGS

(DG-16A)

PIN ARRANGEMENT

CS	1		16	Vec
A _o	2		15	Din
A ₁	3		14	WE
A ₂	4		13	Α,
A ₃	5		12	As
Α.	6		11	Α,
Dout	7	***	10	As
GND	8		9	As
	L			

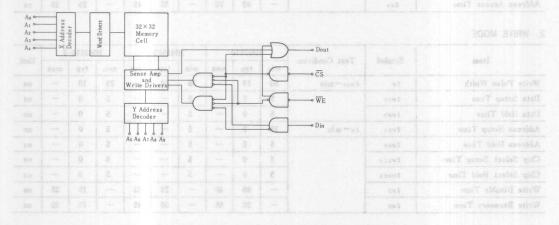
(Top View)

TRUTH TABLE

	Inputs			Vec-6.38V, I10mA
CS	WE	Din	Output	Mode yas dead
Н	X SE	×	Н	Not Selected
L	L	L	Н	Write "0"
L	L	Н	Н	Write "1"
L	Н	×	Dout*	Read

Notes) × : Don't care
* : Read out non-inverted

BLOCK DIAGRAM



BABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2510 Series	Unit
Supply Voltage	Vcc	-0.5 to $+7.0$	V
Input Voltage	Vin	-0.5 to $+5.5$	v
Input Current	Iin	-12 to +5.0	mA
Output Voltage (Output High)	Vout	-0.5 to +5.5	V
Output Voltage (DC Output Low)	Iout	+20	mA
Storage Temperature	Tota	-65 to +150	°C
Storage Temperature	Tota (Bias)*	-55 to +125	°C

^{*} Under Bias

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS ($V_{cc}=5.0V \pm 5\%$, $T_a=0$ to $+75^{\circ}$ C, air flow exceeding 2m/sec)

Item	Symbol		Test Condition			HM2510 Series				
Item	Symbol	lest	Condition	min	typ	max	Unit			
Output Voltage	Vol	Vcc=4.75V, IoL=	16mA	_	0.3	0.45	V			
THURSDON AN	VIH	Guaranteed Input V	oltage High	2.1	1.6		V			
Input Voltage	VIL	Guaranteed Input V	oltage Low	1 -	1.5	0.80	V			
	I 1 H 1	Vcc=5.25V, Vin=4	.5V	_	0	40	μΑ			
Input Current	I 1 H 2	Vcc=5.25V, Vin=5	.25V	_	0	1.0	mA			
	In	Vcc=5.25V, Vin=0).4V	_	-250	-400	μΑ			
Output Leakage Current	ICEX	$V_{CC}=5.25$ V, $V_{out}=$	4.5V	-	0	100	μΑ			
Input Clamp Voltage	V_I	Vcc=5.25V, Iin=-	-10mA	_	-1.1	-1.5	V			
0 1 0	A	Vcc=5.25V	0< Ta < 25°C	111		155	mA			
Supply Current	Icc	All input GND	<i>Ta</i> ≥ 25°C	_	95	130	mA			

•AC CHARACTERISTICS ($V_{cc}=5.0V \pm 5\%$, $T_a=0$ to $+75^{\circ}$ C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	Н	M2510	- 1000.1	HN	12510-	1	Н	M2510-	-2	Uni
Item	Symbol	lest Condition	min	typ	max	min	typ	max	min	typ	max	Uni
Chip Select Access Time	tacs		-	15	40	_	_	30	_	15	25	ns
Chip Select Recovery Time	trcs		-	25	40	_	-	30	1,4-1.0	17	25	ns
Address Access Time	taa		_	40	70	_	35	45	_	25	35	ns

2. WRITE MODE

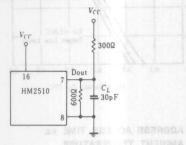
Item	C 1.1	Test Condition		HM251	0	Н	M2510	-1	Н	M2510	-2	11.1
Item	Symbol	lest Condition	min	typ	max	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	twsa=min	50	10	-	35	10	io are	25	10	_	ns
Data Setup Time	twsp	10.00	5	0	1-	5	_	_	5	0	_	ns
Data Hold Time	t wh D		5	0	-	5	3.01	Technical Discosts	5	0	_	ns
Address Setup Time	twsA	tw=min	15	0	-	5	7	1+1	5	0	_	ns
Address Hold Time	t wha		5	0	-	5	37. 4	SUPERIOR	5	0	_	ns
Chip Select Setup Time	twscs		5	0	_	5	_	-	5	0	_	ns
Chip Select Hold Time	twncs		5	0	-	5	-	_	5,	0	-	ns
Write Disable Time	tws		-	20	40	-	20	35	_	15	25	ns
Write Recovery Time	t wn		-	30	55	_	30	45	_	15	25	ns

3. CAPACITANCE

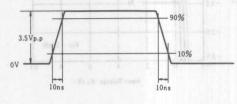
TEMSTICS	OA HO TUNEO	Test Condition	Н	HM2510 Series				
Item	Symbol	lest Condition	min	typ	max	Unit		
Input Capacitance	Cin	· IN-		3	5	pF		
Output Capacitance	Cout		-	6	8	pF		

TEST CIRCUIT AND WAVEFORMS

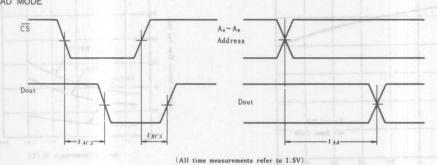
1. LOADING CONDITION



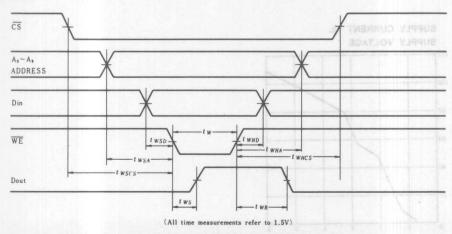
2. INPUT PULSE

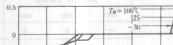


3. READ MODE

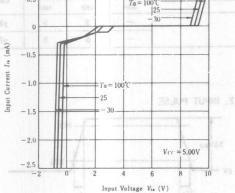


4. WRITE MODE

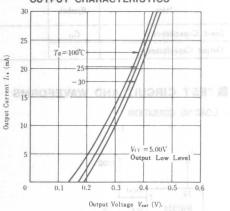




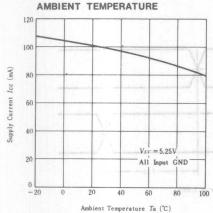
INPUT CHARACTERISTICS



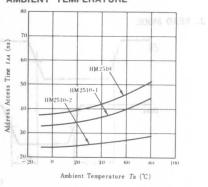
OUTPUT CHARACTERISTICS



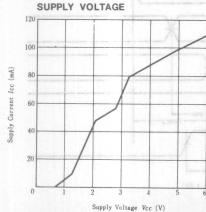
SUPPLY CURRENT vs.



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs.



HM2511, HM2511-1

1024-word×1-bit Fully Decoded Random Access Memory 301731931049410 000

The HM2511 Series item is a 1024-word x 1-bit read/write random access memory with three-state output developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with TTL logic families.

- Level TTL compatible
- Construction 1024-word x 1 bit
- Read access time HM2511: 70ns (max)

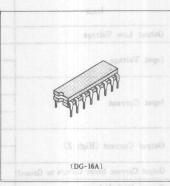
HM2511-1: 45ns (max)

• Chip select access time HM2511: 40ns (max)

HM2511-1: 30ns (max)

Power consumption 0.5mW/bit

Output three-state



PIN ARRANGEMENT

TRUTH TABLE

	Input		0	N. 1
CS	WE	Din	Output	Mode
Н	×	×	High Z	Not Selected
L	L	L	High Z	Write "0"
diall L	L	Н	High Z	Write "1"
L	Н	×	Dout*	Read

Notes) × : Don't care

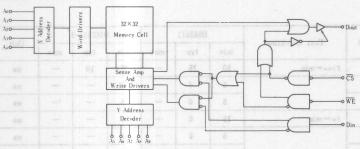
* : Read out noninverted

CS 1 16 Vcc 15 Din 14 WE 13 A, 4 13 A, 5 112 A, 6 111 A, Dout 7 10 A, 6 9 A, 6

(Top View)

2 WHITE MODE

BLOCK DIAGRAM



MADSOLUTE MAXIMUM RATINGS

	75 72 72		
Item	Symbol	HM2511 Series	Unit
Supply Voltage	Vcc	-0.5 to $+7.0$	V
Input Voltage	Vin	-0.5 to +5.5	V
Input Current	Iin	-12 to +5.0	mA
Output Voltage (Output High)	Vout	-0.5 to $+5.5$	V
Output Voltage (DC Output Low)	Iout	+20	mA
Storage Temperature	Tels	-65 to +150	°C
Storage Temperature	Tstg (Bias)*	-55 to +125	°C

* Under Bias

ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (Vcc=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

	C 11	obner stirw\base	sid-f x brow-i	H	M2511 Ser	ies	Unit
Item	Symbol	Test C	ondition	min	typ	max	Unit
Output Low Voltage	Vol	Vcc=4.75V, IoL=	16mA	interior in	0.3	0.45	V
	VIH	Guaranteed Input	Voltage High	2.1	1.6	rition str	V
Input Voltage	VIL	Guaranteed Input	Voltage Low		1.5	0.8	eve_V
	IIH 1	Vcc=5.25V, Vin=	4.5V	in the	0 0	40	μA
Input Current	I 1H 2	Vcc=5.25V, Vin=	5.25V		0	1.0	mA
	IIL	Vcc=5.25V, Vin=	0.4V	_	-250	-400	μA
(7.1.5)	I off 1	Vcc=5.25V, Vont=	800	-,	50	μA	
Output Current (High Z)	I OFF 2	Vcc=5.25V, Vout=	-0.5V		. NOTEC	-50	μA
Output Current Short Circuit to Ground	Ios	$V_{cc} = 5.25 \text{V},$	state-confb	· · · ·		-100	mA
Output High Voltage	Von	$I_{OH} = -10.3 \text{mA}, V$	7cc=5.0V ±5%	2.4	_	_	V
Input Clamp Voltage	Vı	Vcc=5.25V, Iin=	-10mA	_	-1.0	-1.5	V
		Vcc=5.25V	0 ≤ Ta < 25°C	_	Title	155	mA
Supply Current	Icc All input GND		<i>Ta</i> ≥25°C		95	130	mA

•AC CHARACTERISTICS ($V_{cc}=5.0 \text{V } \pm 5\%$, Ta=0 to $+75^{\circ}\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	C	Test Condition	HM2511		HM2511-1			1	17.74
	Symbol	lest Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs	bash	-	15	40		1	30	ns
Chip Select to High Z	tzrcs		_	20	40	_	est Tenino	30	ns
Address Access Time	tan		_	40	70	_	35	45	ns

2. WRITE MODE

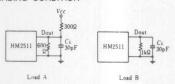
Item	Combal	Test Condition		HM2511		2 - Francis I	HM2511-	1	Unit
Item	Symbol	lest Condition	min	typ	max	min	typ	max	
Write Pulse Width	t w	twsa=min	50	25	1=-	35	10	-	ns
Data Setup Time	twsp		5	0	TTLE	5	_	-	ns
Data Hold Time	t who		5	0	11-	5	_	_	ns
Address Setup Time	twsa	$t_w = \min$	15	0	-	- 5	-	-	ns
Address Hold Time	t wha	-	5	0	- 1	5	_	-	ns
Chip Select Setup Time	twscs		5	0	_	5	_	-	ns
Chip Select Hold Time	twncs		5	0	TAR	5	LAM E	T.U.J.C	ns
Write Disable to High Z	tzws		No.	20	40	-	20	35	ns
Write Recovery Time	t wr	Helf Series III	-	42	55	_	30	45	ns

3. CAPACITANCE

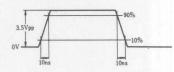
Item	Symbol	Test Condition	HM2511 Series		II-ta	
Item	Symbol	lest Condition	min	typ	max	Unit
Input Capacitance	Cin			3	5	pF
Output Capacitance	Cout		_	9	11	pF

TEST CIRCUIT AND WAVEFORMS

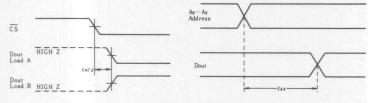
1. LOADING CONDITION



2. INPUT PULSE

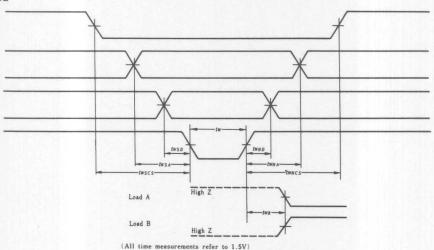


3. READ MODE

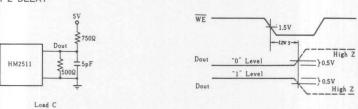


(All time measurements refer to 1.5V)

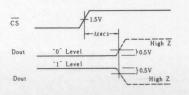
4. WRITE MODE



5. WRITE ENABLE TO HIGH Z DELAY



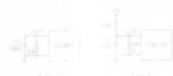
6. PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using Load C)

BITEST CIRCUIT AND WAVEFORMS

LOADING CONDITION



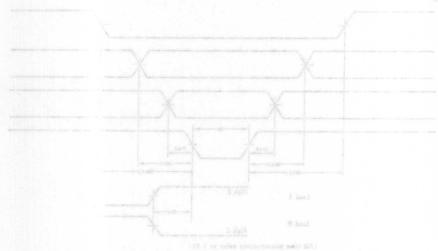


SCHOOL CASE C

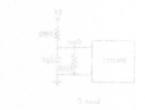


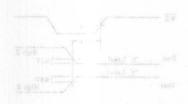
TV2.1 bit within administration with 1.5V7

REDAM STIRW 1

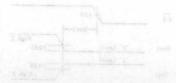


S WRITE ENABLE TO HIGH & DELAY





6. PROPAGATION DELAY PROM CMP SELECT TO HIGH Z



and right off most V2.0 to a 1 m tops (O head 1 tops

REPROCEDENT OF THE STATE OF THE

Filesh is exchargered File Emitter rechnology and programming guise method enables Figher programminglities and fester programmine rene codings PROM cror the Righest edispolities.

Fact prior arming time of typically 7-5 puller is activised with a line sortifier cell which require her programming energy, thus, nephalitis traceral stress. Faction, Hillachi advanced suprolongy allows view highly programmatility.

To service that the alement is programmed properly as additional flow programmed properly as across guidaflow programming unless the applications of the programming subject indicates conduction in the programmed (one programming subject ability from high nothing the programmed subject to the first high nothing sharped only.

The extra new and one extra solume of test cells, glut additional inquity exist into the PROM chip, ellow improved featury taking if DC AC and programming characteristics. Trace not cells and test froutry provide eviltance corrollation between programmed and programmed alreads in order to gustemise high programmability and el-eb-line.

MOTTORS 22090) LIST (SMASS STORE



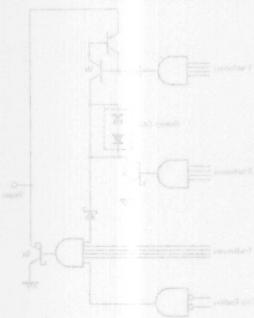
BIPOLAR PROM

The device is manufactured with increase in positive legic "aire"), a pit storage cells. To note which high at a perticular cell, a success in must be changed from a blooking state to a conducting

I logic "one" say be swinters, by measuremed into a sciented bill apparatus for the desired bill for an prantiming is inlected using "est effects inputs to turn on runner is OI and OZ, By tailing that I appear to turn on runner is OI and OZ, By tailing the title of the desired off. Those a train of in regimenting policies applied by the feet of the output flows deep in a practice into sensition OI. This program may current sharpes "grantion to the conducting state, require may be a sensition of a second colories in stopped as social to served colories indicates that the output field the field of the social of the served.

An operational 4 programming policy as \$1 programming pulsas Brandesh are secured to account that it is fully programmed, and to account the high midicality. One or increase the programmed at a time account to insure the instrument decorating or in the capable of similary only one unit of programming current at a construction.

MITERIAL PROGRAMMING ROUT



■ PROGRAMMING INFORMATION

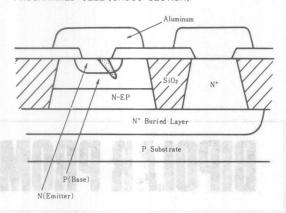
Hitachi's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time ordinary PROMs, for the highest reliability.

Fast programming time of typically $7.5\mu s/bit$ is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Hitachi advanced technology allows very high programmability.

To assure that the element is programmed properly an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed (one programming pulse: Series) bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell.

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and eliability.

PROGRAMMED CELL (CROSS SECTION)

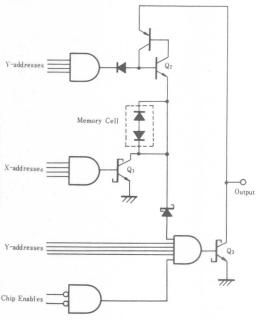


The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using ten address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic in state.

An additional 4 programming pulses (1 programming pulse: S-series) are required to ensure that the bit is fully programmed, and to achieve high reliability. One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at time.

INTERNAL PROGRAMMING CIRCUIT



■ HITACHI PROMS AND PROGRAMMING CURRENT

Memory Size	Organization	Output	N-Series	S-Series
	11.44	0. C.	HN25044 (50ns max)	The HITACHI-HK25004 and I
4k	1k×4	3 S	HN25045 (50ns max)	programmable - Lost decoded
	01 244	O.C.	HN25084 (60ns max)	HN25084S(50ns max)
	2k×4	3 S	HN25085 (60ns max)	HN25085S(50ns max)
8k		o.c. 20	HN25088 (60ns max) HN25088L(100ns max)	HN25088S(50ns max)
	1k×8	3 S	HN25089 (60ns max) HN25089L(100ns max)	HN25089S(50ns max)
101	21.442	O.C.	'ord (fully decoded)	HN25168S(60ns max)
16k	2k×8	3 S	- etiopte	HN25169S(60ns max)
P	rogramming Curren	it	130mA(typ)	90mA(typ)

Note) O.C.: Open Collector Output 3 S: Three State Output

Hitachi's PROM has two families in accordance with the program specifications. They are usually discriminated by the suffix of the model name. For the S-series PROM, the production technique established for the N-series PROM is further improved to attain very small memory cell area and chip area as well as high performance.



HN25044, HN25045

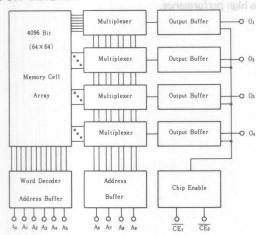
1024-word×4-bit Programmable Read Only Memory
The HITACHI HN25044 and HN25045 are high speed electrically
programmable, fully decoded TTL Bipolar 4096 bit read only
memories organized at 1024 words by 4 bits with on-chip address
decoding and two chip enable inputs. The HN25044 and HN25045
are fabricated with logic level "zeros" (low); logic level "ones"
(high) can be electrically programmed in the selected bit locations.
The same address inputs are used for both programming and reading.

PROTECT STATE (DG-18)

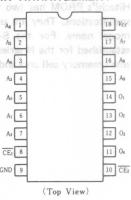
FEATURES

- 1024 words x 4 bits organization (fully decoded)
- TTL Compatible inputs and outputs
- Fast read access time; 30 ns typ. (50 ns max.)
- Medium power consumption; 500 mW typ.
- Two Chip enable inputs for memory expansion
- Open collector outputs (HN25044)/Three-state outputs brooms in political ow (HN25045)
- Standard cerdip 18-pin package

BLOCK DIAGRAM



PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to $+7.0$	V
Input Voltage	Vin	-0.5 to $+5.5$	V
Output Voltage	Vout	-0.5 to $+5.5$	V
Output Current	Iout	50	mA
Operating Temperature	T_{opr}	-25 to +75	°C
Storage Temperature	Tate	-65 to +150	°C

■ DC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to +75°C) TAOPHOSES DHIMMARDORS

Item	cull ₁₋₁	Total Control		HN2504	4 deixel		HN2504	5	Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	inoidm?
	VIH		2.0	-	-	2.0	ilse	N solos	V
Input Voltage	VIL	130元分标	-	-	0.8	-	_	0.8	V
Output Voltage	Von	$I_{OH} = -2\text{mA}$	-	-	-	2.4	-	Salley Land	V
	Vol	$I_{OL} = 16 \text{mA}$	-	-	0.45	-	_	0.45	V
	IIH	$V_{IH} = 2.7 \text{V}$	-	-	40	-	-	40	μA
Input Current	IIL	$V_{IL} = 0.4 \text{V}$	-	-	-0.4	-	-	-0.4	mA
0	- di	Vout = 5.5V	-	-	100	-	-	100	illoniA
Output Leakage Current	IOLK	$V_{out} = 0.4 \text{V}$	-	-	40	_	_	40	μA
Input Clamp Voltage	V_I	$I_{in} = -18 \text{mA}$	inger id er	mati— b	-1.2	d ning	orra lo i	-1.2	V
Power Supply Current	Icc	Input Either Open or at Ground	-	100	130	_	100	130	mA
Output Short-circuit Current	Ios	$V_{out} = 0 \text{ V}$	-	II ban	mstye 10	15	30	60	mA
Input Capacitance	Cin	$V_{in}=2V$, $V_{CC}=0V$	e enoled	5	10	750 70	5	10	pF
Output Capacitance	Cout	$V_{out} = 0 \text{ V}, V_{CC} = 0 \text{ V}$	-	7	12	_	7	12	pF

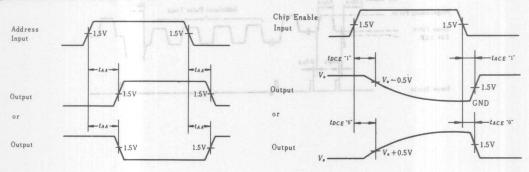
AC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to 75°C)

Item	Symbol	min	typ	max	Unit
Address Access Time	taa	46-N	35	50	ns
Chip Enable Access Time	t ACE	_	20	30	ns
Chip Enable Disable Time	t DCE	-	20	30	ns

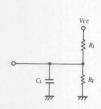
Notes: 1. Typ. value is at V_{CC} =5.0 V and T_a = 25° C

Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5 V from the active output level.

SWITCHING WAVEFORMS



SWITCHING TIME TEST CONDITIONS



SWITCHING		HN25044		HN25045			
PARAMETER	R_1	R ₂	CL	R_1	R2	CL	
taa	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
tACE "1"	_	_	_	00	600Ω	10pF	
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF	
t DCE "1"	-		-	00	600Ω	30pF	
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF	

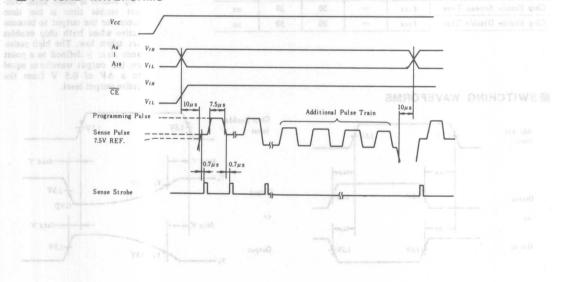
INPUT CONDITIONS
Amplitude - 0V to 3V

Rise and Fall time - 5ns from 1V to 2V Frequency - 1MHz

■ PROGRAMMING SPECIFICATION (# 60 80%) V68.8 (# 87.8 + 60 87.8 +

	Charac	teristic				Limit	Unit	Notes
Ambient Temperature	mars	XSm	Q12	akes .		25±5	°C	
Programming Pulse	0.3	127		0.5			WA	Inout Vultage
Amplitude						130±5%	mA	3883
Clamp Voltage						20+0%-2%	V	
Ramp Rate						70max	V/µs	Outont Voltinge
Pulse Width						7.5±5%	μs	10V point/150Ω load
Duty Cycle						70% min		
Sense Current	-	1.0-	-			Va.der.ch	In	
Amplitude						20±0.5	mA	
Clamp Voltage						20+0%-2%	van V	Ontgot Leakage Caryoni
Ramp Rate						70max	V/µs	10V point/150Ω load
Sense current interr	uption l	pefore a	nd after	address	change	10min	μs	Typet Clamp Veltuge
Programming Vcc	-	136	eor	-	- keessil	5.0+5%-0%	yal V	Power Supply Carront
Maximum Sensed Volta	ge for	program	med "1	"		7.5±0.1	V	Output Shert-eineut Omeren
Delay from trailing edg	e of pr	ogrammi	ng pulse	e before s	sensing	Vomesty Vomesty	m3	Input Caparibases
output voltage	14	NI.				0.7min	μs	Ground Connectioner
Programming Time All	ocation	/Bit	Sinte			100max	ms	
Additional Programmin	g Pulse	Number	-	C-YAS	- A	4	Time	DETTARASA SAE

TYPICAL WAVEFORMS

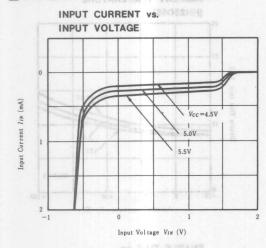


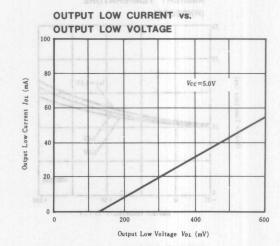
ESWITCHING TIME TEST CONDITIONS

SWITCHING					
	3000				
"I" and					
		6000		0.000	
		51009		0000	

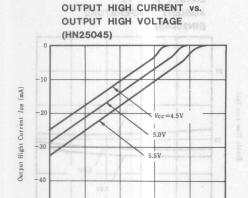


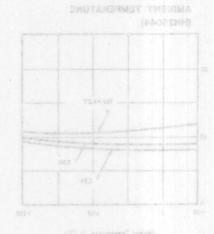
TYPICAL DC CHARACTERISTICS





DISABLE TIME VS

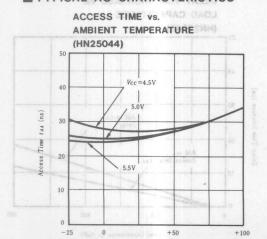


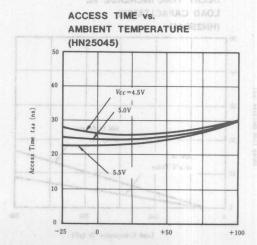


TYPICAL AC CHARACTERISTICS

Output High Voltage Von (V)

-50



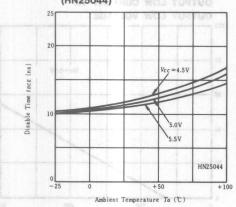


Ambient Temperature Ta (°C)

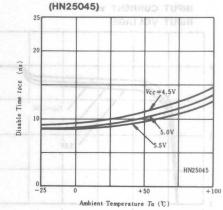
OHITACHI

DISABLE TIME vs.

AMBIENT TEMPERATURE
(HN25044) AMD WOLLTUSTUO

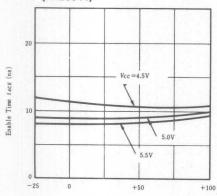


DISABLE TIME vs. AMBIENT TEMPERATURE



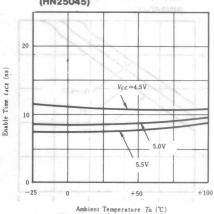
ENABLE TIME vs.

AMBIENT TEMPERATURE
(HN25044)



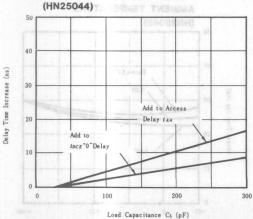
ENABLE TIME vs.

AMBIENT TEMPERATURE
(HN25045)

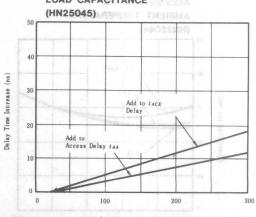


Ambient Temperature Ta (°C)

DELAY TIME INCREASE vs. LOAD CAPACITANCE



DELAY TIME INCREASE vs.



HN25084, HN25085

2048-word×4-bit Programmable Read Only Memories

The HITACHI HN25084 and HN25085 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 word by 4 bit with on-chip address decoding and one chip enable input. The HN25084 and HN25085 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 2048 word x 4 bit organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084)/Three-state outputs (HN25085)
- Standard cerdip 18-pin dual in-line package

■ OPERATION

Programming

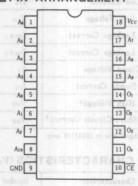
A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing CE to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

Reading

To read the memory the device is enabled by bringing \overline{CE} to a logic "zero". The outputs then correspond to the data programmed in the selected word.

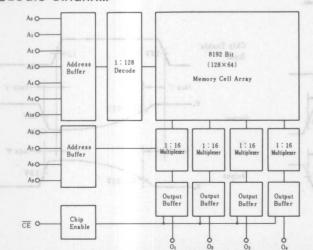
(DG-18)

PIN ARRANGEMENT



(Top View)

LOGIC DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to $+7.0$	ga deV
Input Voltage	Vin	-0.5 to $+5.5$	V
Output Voltage	Vout	-0.5 to $+5.5$	V
Output Current	Iout	50	mA
Operating Temperature	Topr	-25 to +75	°C
Storage Temperature	Tota	-65 to +150	°C

DC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to 75°C)

					- 25 TE CLE	270 A 71 D 92
Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	V_{IH}	23	2.0	estu çi ni i	or np atible	V
Input Low Voltage	VIL	(80 ns max)	ns_eyp.	Wares &	0.8	V
Input High Current	IIH	V ₁ =2.7V	idd t <u>n</u> ell	elumation of	40	μA
Input Low Current	-In	V _I = 0.4V	anac Mu	STUTTUE	0.40	mA
Output Low Voltage	Vol	$I_{OL} = 16 \mathrm{mA}$	_	_	0.45	V
Output Leakage Current	IOLKI	Vo=5.25V soakoo e	iil mHs :-	li niq-81	100	μΑ
Output Leakage Current	I OLK 2	Vo=0.4V	_		40	μΑ
Input Clamp Voltage	V_I	$I_t = -18 \text{mA}$	_	_	-1.2	V
Power Supply Current	Icc	Inputs Either Open or at Ground	Vunne	110	150	mA
Output High Voltage*	Von	$I_0 = -2 \text{mA}$	2.4	alpha gan	d filmen Ac	V
Output Short Circuit Current*	-Ios	Vo=0V to misst a medit meno" o	15	Bit-en	60	mA

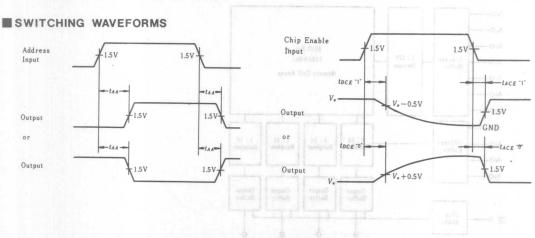
^{*} Note: Applicable to HN25089 only.

■ AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	taa	nebled by bringing CE to a logic	si soive	40	60	ns
Chip Enable Access Time	tACE	are the demandered and on the	lods? vor	25	35	ns
Chip Enable Disable Time	t DCE		_	25	35	ns

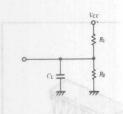
Note) 1. Output Load: See Test Circuit.

2. Measurement Reference: 1.5V for both inputs and outputs.



■ Fast read eccest time: 26 ns typ. (60 ns max)

SWITCHING TIME TEST CONDITIONS



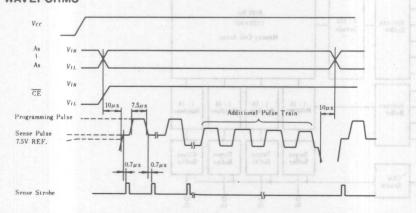
SWITCHING	Hmort	IN25084	O bas	ole Fil	HN25085	
PARAMETER	R_1	Rz	CL	R_1	Rz	CL
taa	300Ω	600Ω	30pF	300Ω	600Ω	.30pF
tace "1"	enubs i	HI30-130	rutts e	00	600Ω	10pF
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t DCE "1"	no il soc	i sid b	salecte	00	600Ω	30pF
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude - OV to 3V
Rise and Fall time - 5ns from 1V to 2V
Frequency - 1MHz

PROGRAMMING SPECIFICATION

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	80g2 .C	Pen conector curp
Programming Pulse Amplitude Clamp Voltage Ramp Rate Pulse Width Duty Cycle	7004	mA V V/μs μs	-8f albus outlines 4 MOLTARIS 10 III gnimmorgus 2 10V point/150Ω load A
Sense Current Amplitude Clamp Voltage Ramp Rate Sense Current Interruption before and after address char	20±2% 70max	mA V V/μs μs	selected by the ran disabled by bringing ourrent programming the sensed volvage indi-
Programming Vcc	5.0+5%-0%	V	Paging of additional puri
Maximum Sensed Voltage for programmed "1"	7.5±0.1	na si soi V b e	
Delay from trailing edge of programming pulse before sensi	ng 0.7min	μς	"zero". The outputs ti-
Programming Pulse Number	100max	ms	
Additional Programming Pulse Number	4	Time	MARDAIG DIDOJEM

TYPICAL WAVEFORMS



HN25084S, HN25085S

2048-word×4-bit Programmable Read Only Memories

The HITACHI HN25084S and HN25085S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 words by 4 bits with on-chip address decoding and one chip enable input. The HN25084S and HN25085S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 2048 words x 4 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084S)/Three-state outputs (HN25085S)
- Standard cerdip 18-pin dual in-line package.

OPERATION

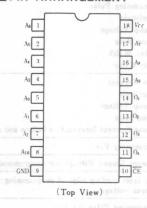
Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing $\overline{\text{CE}}$ to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

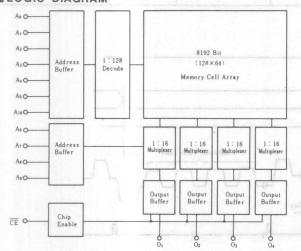
Reading

To read the memory the device is enabled by bringing $\overline{\text{CE}}$ to a logic "zero". The outputs then correspond to the data programmed in the selected word.

PIN ARRANGEMENT



LOGIC DIAGRAM





BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	Vin OB	-0.5 to +5.5	V
Output Voltage	Vout	-0.5 to +5.5	V
Output Current	Iout	50,00	mA
Operating Temperature	Topr	-25 to +75	°C
Storage Temperature	Tare	-65 to +150	°C

DC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to 75°C)

Characteristic	Symbol	Te	st Condition	ns	min	typ	max	Unit
Input High Voltage	V_{IH}			940	2.0	ege o	ENDER	V
Input Low Voltage	VIL			Landar D	-	02252	0.8	V
Input High Current	I _{1H}	V1-2.7V		To Addition to the second	-	-	40	μA
Input Low Current	$-I_{IL}$	$V_I = 0.4 \text{V}$	10. 1				0.40	mA
Output Low Voltage	Vol	I o = 16mA				_	0.45	V
Output Leakage Current	IOLKI	$V_o = 5.25 \text{V}$	88	I o	_	-	100	μА
Output Leakage Current	IOLK 2	$V_o = 0.4 \text{V}$	0.01	al al	-		40	μА
Input Clamp Voltage	V_I	$I_I = -18 \text{mA}$	1.5		-	-	-1.2	V
Power Supply Current	Icc	Inputs Either	Open or at	Ground	-	110	160	mA
Output High Voltage*	Von	$I_o = -2 \text{mA}$			2.4	_	Jan 93	SaVse C
Output Short Circuit Current*	$-I_{os}$	Vo=0V	61		15	-	60	mA

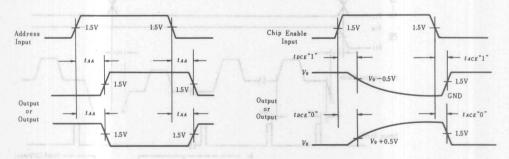
^{*} Note: Applicable to HN25089 only.

AC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	taa	1.0	-	25	50	ns
Chip Enable Access Time	tACE		-	20	35	ns
Chip Enable Disable Time	t DCE		- Jul 40	15	35	ns

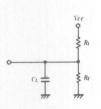
Note) 1. Output Load: See Test Circuit.

SWITCHING WAVEFORMS



^{2.} Measurement Reference: 1.5V for both inputs and outputs.

SWITCHING TIME TEST CONDITIONS



SWITCHING	MaUI	HN25084	S malast	HN25085S			
PARAMETER	R_1	R ₂	CL	R_1	R2	CL	
t AA	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
t ACE "1"	2	1-8	2+ ==	00	600Ω	10pF	
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF	
t DCE "1"	170	-8	1+ 0+ 8	00	600Ω	30pF	
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF	

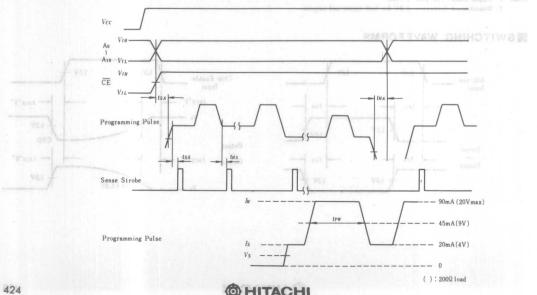
INPUT CONDITIONS

Amplitude-0V to 3V
Rise and Fall time-5ns from 1V to 2V

 ${\tt Frequency-1MHz}$

■ PROGRAMMING SPECIFICATION

PARAME	TER		Symbol	min	typ	max	Unit	Note
Ambient Temperature			Ta	20	25	30	°C	maranta dili meni
Programming Vcc			Vcc	4.75	5.0	5.25	V	marine and impri
Programming Pulse Amplitude	-		Iw	88	90	92	mA	Curpor Low Suringo
Clamp Voltage Ramp Rate Pulse Width			Vw t pw	19.0 10 7.1	19.5 - 7.5	20.0 70 7.9	V V/μs μs	9V point/200Ω load
Duty Cycle	110		hoson	70	rodii li alsa	inf no i	%	Power Supply Current
Sense Current Amplitude Sense Voltage		k.0	Is Vs	19 7.4	20 7.5	21 7.6	mA V	Output High Voltage*
Clamp Voltage Ramp Rate				19.0 70	19.5	20.0	V V/μs	More Applicable to MICEL
Address Setup Time			tsa	10	5'02'10 00 c	K. 6 52 A. 1	μs	HUAMAND DAR
Address Hold Time	d41	alm	t HA	10	T . T	Symplect .	με	Characteristic
Sense Setup Time Sense Hold Time			tss ths	0.7 0.7	=	_ 44.1	μs μs	Address Access Time
Additional Programmin	g Pulse			1	1	122.1	time	Onip Smable Access To
Programming Pulse Nu	mber pe	er bit	n		_	10000	time	Chip Enghie Divible I'i



HN25088, HN25089

1024-word×8-bit Programmable Read Only Memories

The HITACHI HN25088 and HN25089 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088 and HN25089 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.



- 1024 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 40 ns (typ), 60 ns (max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088)/Three-state outputs (HN25089)
- Standard cerdip 24-pin dual in-line package

■ OPERATION

Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing CE1 and/or CE2 to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

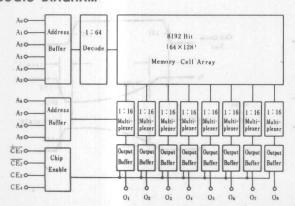
To read the memory the device is enabled by bringing CE1 and CE2 to a logic "zero". CE3 and CE4 to a logic "one". The outputs them correspond to the data programmed in the selected word.

(DG-24)

PIN ARRANGEMENT



LOGIC DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	e do V
Input Voltage	Vin	-0.5 to +5.5	Q878v islo
Output Voltage	Vout	-0.5 to +5.5	TO PAY VIIIC
Output Current	Iout	50	mA
Operating Temperature	Topr	-25 to +75	°C
Storage Temperature	Tota	-65 to +150	°C

DC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to $+75^{\circ}$ C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	VIH	2118	2.0	aruq n i s	diteamo	V
Input Low Voltage	VIL), 60 ns (max)	O n <u>s.</u> (cyc	A complete	0.8	V
Input High Current	IIH	$V_t = 2.7 \text{V}$	30 : <u>no</u> 110	900 Sture	40	μA
Input Low Current	$-I_{IL}$	V ₁ =0.4V	HILLIAND SECOND	SECULIAR SE	0.40	mA
Output Low Voltage	Vol	$I_{OL} = 16 \mathrm{mA}$		_	0.45	V V
Output Leakage Current	I OLK 1	V ₀ =5.25V	E-ni teub	gio ti S	100	μΑ
Output Leakage Current	IOLK2	Vo=0.4V	_	-,	40	μΑ
Input Clamp Voltage	Vi	$I_I = -18 \text{mA}$	_	_	-1.2	NO TO
Power Supply Current	Icc	Inputs Either Open or at Ground	-	120	160	mA
Output High Voltage*	Von	$I_{OH} = -2 \mathrm{m}\mathrm{A}$	2.4	misq so	THE CHE	V
Output Short Circuit Current*	-Ios	V ₀ =0V	15	thine out	60	mA

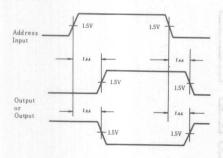
^{*} Note: Applicable to HN 25089 only.

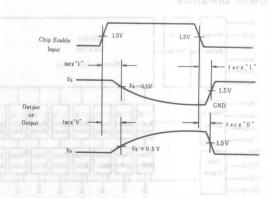
EAC CHARACTERISTICS $(V_{cc}=4.75 \text{ to } 5.25\text{V}, T_a=0 \text{ to } 75^{\circ}\text{C})$

Characteristic	Symbol	Test Conditions	min 18	typ	max	Unit
Address Access Time	taa	hen is stopped.	spp <u>H</u> ad, t	40	60	ns
Chip Enable Access Time	tACE			20	35	ns
Chip Enable Disable Time	t DCE	Maked by bringing ce a and clea	0.21 83172	20	35	ns

Note) 1. Output Load: See Test Circuit.

SWITCHING WAVEFORMS

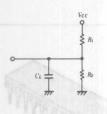




^{2.} Measurement Reference: 1.5V for both inputs and outputs.

TTL compatible inputs and outputs

SWITCHING TIME TEST CONDITIONS



SWITCHING		HN25088	O bae	HN25089			
PARAMETER	R_1	R2	CL	R_1	R ₂	CL	
taa	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
tace "1"	8 200 8 200	rae <u>u</u> u	pri T	∞	600Ω	10pF	
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF	
t DCE "1"	bernel	SIZ COTA	ni ben	00	600Ω	30pF	
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF	

INPUT CONDITIONS

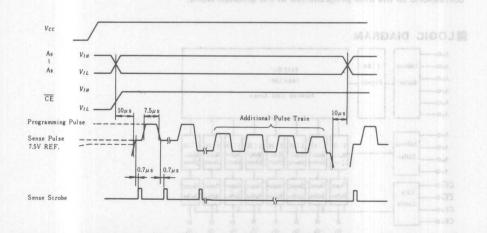
Amplitude - 0V to 3V

Rise and Fall time - 5ns from 1V to 2V

Frequency - 1MHz

■ PROGRAMMING SPECIFICATION

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	ni eldane giro nuo-i
Programming Pulse	SVThree-state outp	uts (HN2508	Open collector outp
Amplitude	130±5%	mA	(200025004)
Clamp Voltage	20±2%	V.	Standard cerdip 24
Ramp Rate	70max	V/µs	TAS MINITED TO DESCRIPTION OF THE
Pulse Width	7.5±5%	μs	10V point/150Ω load
Duty Cycle	70% min		BOPERATION
Sense Current			o Programming
Amplitude 110 betaal 32	20±0.5	mA	A logic one can by p
Clamp Voltage	20±2%	lans galymen	location by using pro-
Ramp Rate	70max	V/µs	ner out yo beroales
Sense Current Interruption before and after address change	10min	To\tan µs 3	gragaind ye baldsalb
Programming Vcc in the region of the region	5.0+5%-0%	de Asero.	and/or CEA to a lo
Maximum Sensed Voltage for programmed "1"	7.5±0.1	OF DEFEVE	programming pulser
Delay from trailing edge of programming pulse before sensing output voltage	0.7min	balla µs	s of seluq fanottibbs no
Programming Pulse Number	100max	ms	Various the suspense
Additional Programming Pulse Number	4.1	Time	130 "ones" dieni sint



HN25088S, HN25089S

The HITACHI HN25088S and HN25089S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit-read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088S and HN25089S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088S)/Three-state outputs (HN25089S)
- Standard cerdip 24-pin dual in-line package

■ OPERATION

Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing CET and/or CE2 to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

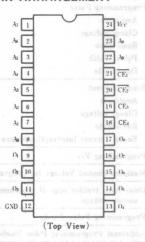
Reading

To read the memory the device is enabled by bringing CE1 and CE2 to a logic "zero", CE3 and CE4 to a logic "one". The outputs then correspond to the data programmed in the selected word.

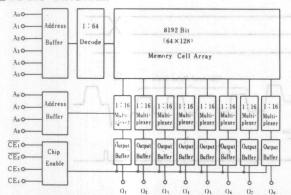
(DG-24)

PIN ARRANGEMENT

SWITCHING TIME TEST CONDITIONS



LOGIC DIAGRAM



WSWITCHING TIME TEST CONDITIONS

MADE ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	02 Vin 000	-0.5 to +5.5	o V
Output Voltage	Vout	-0.5 to +5.5	V
Output Current	I out	C 308 Tg01 50 G	mA
Operating Temperature	Topr 10	-25 to +75	°C
Storage Temperature	C Tets	-65 to +150	.C

DC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to $+75^{\circ}$ C)

Characteristic	Symbol	Tes	st Conditions	3	min	typ	max	Unit
Input High Voltage	V_{IH}			NO	2.0	pane or	amea,s	DO N
Input Low Voltage	VIL	0.004	41.00	Lodově	-	9.7773	-0.8	v
Input High Current	I _{IH}	V1-2.7V	ne		-	-	40	μA
Input Low Current	-IIL 30	$V_I = 0.4 \text{V}$	25	100	-	-	0.40	mA
Output Low Voltage	Vol	$I_{OL} = 16 \mathrm{mA}$			-	-	0.45	v
Output Leakage Current	IOLK 1	Vo=5.25V	.88	91	- 1	-	100	μA
Output Leakage Current	IOLK 2	$V_o=0.4V$	0.61	94	-	m-1	40	μA
Input Clamp Voltage	VI ex	$I_I = -18 \text{mA}$	1.7	well.	-		-1.2	V V
Power Supply Current	Icc	Inputs Either (Open or at C	Fround	_	120	160	mA
Output High Voltage*	Von	$I_{OH} = -2 \mathrm{mA}$			2.4	-	in t	V
Output Short Circuit Current*	-Ios	$V_o = 0$ V	4.5	. 9	15	-	60	mA

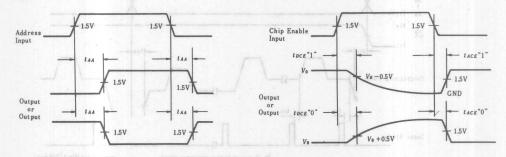
^{*} Note: Applicable to HN25089S only.

AC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t AA	1.0	-	25	50	ns
Chip Enable Access Time	tACE			20	35	ns
Chip Enable Disable Time	t DCE COO	n	Tild 1	15	35	ns

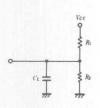
Note) 1. Output Load: See Test Circuit.

SWITCHING WAVEFORMS



^{2.} Measurement Reference: 1.5V for both inputs and outputs.

SWITCHING TIME TEST CONDITIONS



SWITCHING	not I	HN25088	S . satisfa	I	HN25089	3	
PARAMETER	Ri	R ₂	CL	R_1	R2	CL	
taa	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
tace "1"	-	-	801	00	600Ω	10pF	
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF	
t DCE "1"	-	-	5 - 12	00	600Ω	30pF	
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
						-	

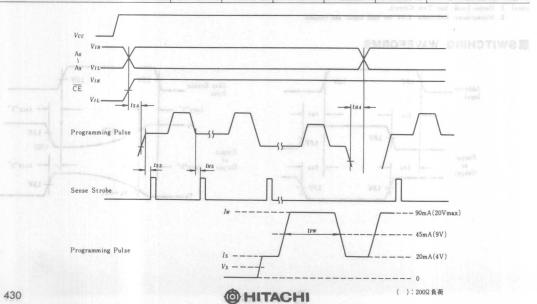
INPUT CONDITIONS

Amplitude - OV to 3V
Rise and Fall time-5ns from 1V to 2V

Frequency-1MHz

■ PROGRAMMING SPECIFICATION

PARAMET	ER		Symbol	min	typ	max	Unit	Note
Ambient Temperature			Ta	20	25	30	°C	Input Edgi Current
Programming Vcc			Vcc	4.75	5.0	5.25	V	legist Los Carrest
Programming Pulse		1550			Ambr-	POP 1 792		Outgut Low Voltage
			Iw	88	90	92	mA	Output Lealings Correct
Clamp Voltage Ramp Rate			Vw	19.0 10	19.5	20.0	V V/μs	Output Leakage Courses
Pulse Width			t pw	7.1	7.5	7.9	μs	9V point/200Ω load
Duty Cycle			States	70	ne Esther Op	and - and	%	Power Supply Carrent
Sense Current	4	2.5			Ams	Fair Los		Output High Voltage*
Amplitude			Is	19	20	21	mA	
Sense Voltage			Vs	7.4	7.5	7.6	V	Outget Shart Circuit Car
Clamp Voltage				19.0	19.5	20.0	V	S. Note : Applicable to ENTROPY
Ramp Rate				70	-	- 1	V/µs	
Address Setup Time			tsA	10	V65. 8_01	$\Pi_{-k} = \underline{\iota}_{-k}(V)$	μs	MARAGO DA M
Address Hold Time			t HA	10	-	Today	μs	Situates estated
Sense Setup Time			tss	0.7	_		μs	The second secon
Sense Hold Time			tHS	0.7	_	- 111	μs	Adlesas Accass Time
Additional Programming	Pulse			1	1	100	time	Chip Ebable Accord Ture
Programming Pulse Num	ber per	r bit	n	_	-	10000	time	Cidg Lable Double The



HN25088L, HN25089L

1024-word × 8-bit Programmable Read Only Memories

The HITACHI HN25088L and HN25089L are low power and high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 1024 words by 8 bits with onchip address decoding and four chip enable inputs.

The HN25088L and HN25089L are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 60ns typ. (100ns max.)
- Low power consumption: 350mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088L)/Three-state outputs (HN25089L)

■ OPERATION

Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing CE1 and/or CE2 to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory the device is enabled by bringing CE1 and CE2 to a logic "zero", CE3 and CE4 to a logic "one". The outputs then correspond to the data programmed in the selected word.

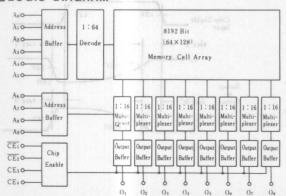
(DG-24)

PIN ARRANGEMENT



MISWITCHING WAVEFORMS

LOGIC DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V V
Input Voltage	Vin	-0.5 to +5.5	V
Output Voltage	Vout	-0.5 to +5.5	yd alvoy
Output Current	Iout	50	mA
Operating Temperature	T_{opr}	-25 to +75	°C
Storage Temperature	Tets	-65 to +150	°C

DC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to $+75^{\circ}$ C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Y	V_{IH}	211	2.0	MILION S	rtinamo	V
Input Voltage	V_{IL}	p. (100ns mex.)	Stris ty	s tivne:	0.8	Vest
0	V _{OH} *	$I_{OH} = -2 \mathrm{mA}$	2.4	girq - nusi	ower cor	VOV
Output Voltage	Vol	IoL=16mA	mem_ioi	aru <u>u</u> u si	0.45	v
	I_{IH}	V_{I} = 2.7V	u) sinc	200 10	40	μA
Input Current	$-I_{IL}$	$V_I = 0.4 \text{V}$	_	(3000)	0.4	mA
0		$V_0 = 5.25 \text{V}$	_		100	
Output Leakage Current	IOLK	$V_0 = 0.4 \text{V}$	_	_	40	μΑ
Supply Current	Icc	Inputs Either Open or at Ground	_	70	100	mA
Output Short-circuit Current	-Ios*	Vo=0V	8	inte pari	30	mA
Input Clamp Voltage	V_I	$I_I = -18\mathrm{mA}$	Bas Buru	пак фото	-1.2	V

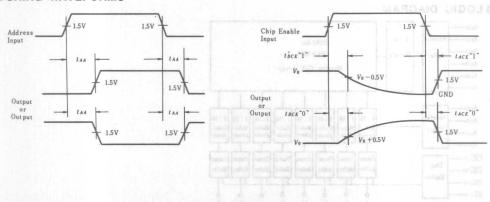
^{*} Applicable to HN25089L only.

\blacksquare AC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to $+75^{\circ}\mathrm{C}$)

Item	Symbol	min	typ	max	Unit
Address Access Time	tAA	stopper	ei ner 60 balles	100	ns ns
Chip Enable Access Time	tACE		40	70	ns
Chip Enable Disable Time	t _{DCE}	by bringing C	40	eb 9/1/70 om	ns

Notes) 1. Output Load: See Test Circuit

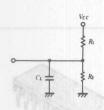
SWITCHING WAVEFORMS



^{2.} Measurement Reference: 1.5V for both inputs and outputs

* 2048 words x 8 bits organization (fully decoded)

SWITCHING TIME TEST CONDITIONS



SWITCHING	nome	IN250881	O bar	He R	HN250891	Progra	hid-8 x brow-85
PARAMETER	R_1	R2	CLI	R_1	R ₂	CL	
taa	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
t ACE "1"	29 (10) <u>D</u> E	QINQ-IR	DIW	00	600Ω	10pF	
tACE "O"	300Ω	600Ω	10pF	300Ω	600Ω	10pF	
t DCE "1"	id bases	alea ori	ol be	00	600Ω	30pF	ed and (dpid) "se
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF	tions. The same ad

INPUT CONDITIONS

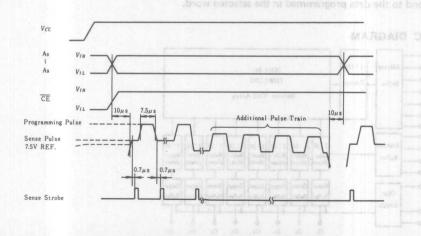
Amplitude - 0V to 3V

Rise and Fall time - 5ns from 1V to 2V

Frequency - 1MHz

■ PROGRAMMING SPECIFICATION

Characteristic		Limit	Unit	Notes
Ambient Temperature		25±5	°C	Three cities and a
Programming Pulse Amplitude Clamp Voltage Ramp Rate Pulse Width Duty Cycle	2100	$130\pm5\%$ $20\pm2\%$ $70_{\rm max}$ $7.5\pm5\%$ 70% min	mA V V/μs μs	10V point/150Ω load
Sense Current Amplitude Clamp Voltage Ramp Rate Sense Current Interruption before and	after address change	20±0.5 20±2% 70max 10min		e Programming A logic one can bu p location by using program is selected by the ele-
Programming Vcc	ang pulsos is	5.0+5%-0%	doirl to Vrisit	logic "zero", Then a
Maximum Sensed Voltage for programme	d "1" for aersolon	7.5±0.1	restA J v mus	applied to the desired
Delay from trailing edge of programming output voltage	pulse before sensing	0.7min	μs	the solected bit is applied, then is stopped
Programming Pulse Number	1000	100max	ms	e Reading
Additional Programming Pulse Number	DIED: 0 0) 121	guigaria ye belasi	Time	To read the memory to



HN25168S, HN25169S

2048-word×8-bit Programmable Read Only Memories The HITACHI HN25168S and HN25169S are high speed electrically programmable, fully decoded TTL Bipolar 16384 bit read only memories organized as 2048 words by 8 bits with on-chip address decoding and three chip enable inputs. The HN25168S and HN25166S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 2048 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 600 mW typ.
- Three chip enable inputs for memory expansion.
- Open collector outputs (HN25168S)/Three-state outputs (HN25169S)
- Standard cerdip 24-pin dual in-line package

■ OPERATION

Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired world is selected by the eleven address inputs in TTL level. The device is disabled by bringing CE1 to as logic "one" or CE2 and/or CE3 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse is applied, then is stopped.

Reading

To read the memory the device is enabled by bringing CE1 to a logic "zero", CE2 and CE3 to a logic "one". The outputs then correspond to the data programmed in the selected word.

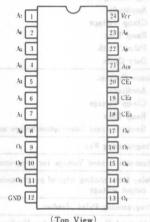
A6 2

(Top View)

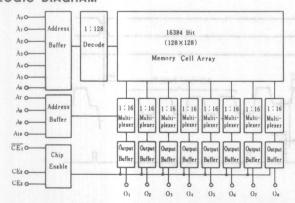
PIN ARRANGEMENT

(DG-24)

PROGRAMMING SPECIFICATION



LOGIC DIAGRAM



MADSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	S Via sol	-0.5 to +5.5	V.
Output Voltage	Vout	-0.5 to +5.5	V
Output Current	I out	50 00	mA
Operating Temperature	T_{opr}	-25 to +75	°C
Storage Temperature	Tate	-65 to +150	.c

DC CHARACTERISTICS ($V_{cc}=4.75$ to 5.25V, $T_a=0$ to $+75^{\circ}C$)

Characteristic	Symbol	Tes	st Conditions	DUAL TO	min	typ	max	Unit
Input High Voltage	V_{IH}			-MOIT	2.0	ege=oH	EMMAR.	V
Input Low Voltage	Vil			4-49	-	-	0.8	v
Input High Current	Іін	$V_I = 2.7 \text{V}$	460		-		40	μA
Input Low Current	-111	$V_I = 0.4 \text{V}$	92.4	-31	-	_	0.40	mA
Output Low Voltage	Vol	$I_{OL} = 16 \mathrm{mA}$			-	-	0.45	V
Output Leakage Current	IOLKI	Vo=5.25V	88	w.l.	-	-	100	μA
Output Leakage Current	IOLK 2	Vo=0.4V	0.61	48		-	40	μΑ
Input Clamp Voltage	V _I	$I_{i} = -18 \text{mA}$	1.5	nen û	-	-	-1.2	V
Power Supply Current	Icc	Inputs Either (pen or at G	round	-	120	170	mA
Output High Voltage*	Von	$I_{OH} = -2 \mathrm{m}\mathrm{A}$			2.4	-	1000	V
Output Short Circuit Current*	-Ios	Vo-0V	1	11	15	-	60	mA

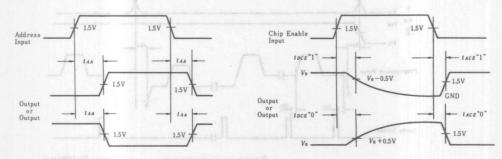
^{*} Note: Applicable to HN25169S only.

AC CHARACTERISTICS $(V_{cc}=4.75 \text{ to } 5.25\text{V}, T_a=0 \text{ to } 75^{\circ}\text{C})$

Characteristic	Symbol	Test Conditions	1		amiX Joid	Unit
Characteristic	Symbol	lest Conditions	min	typ	max	Unit
Address Access Time	t AA		-	40	60	ns
Chip Enable Access Time	tACE		-	20	35	ns
Chip Enable Disable Time	t DCE	- 1	-nd	20	35	ns

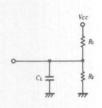
Note) 1. Output Load: See Test Circuit.

SWITCHING WAVEFORMS



^{2.} Measurement Reference: 1.5V for both inputs and outputs.

SWITCHING TIME TEST CONDITIONS



SWITCHING	Jan H	IN251685	S solra	HN25169S		
PARAMETER	R_1	R2	CL	R_1	R ₂	CL
taa	300Ω	600Ω	30pF	300Ω	600Ω	30pF
tace "1"	4	-	(c- + 5)	00	600Ω	10pF
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t DCE "1"		-	(+ a) (- 00	600Ω	30pF
t DCE "0"	300Ω	600Ω	30pF	300Ω	600₽	30pF

INPUT CONDITIONS

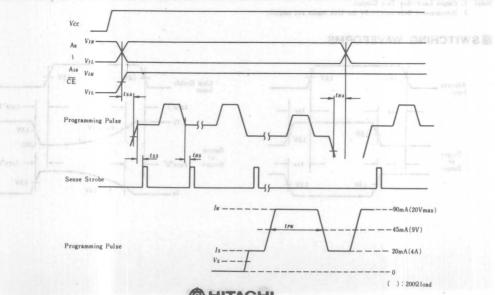
Amplitude - 0V to 3V

Amplitude-0V to 3V Rise and Fall time-5ns from 1V to 2V

Frequency-1MHz

■PROGRAMMING SPECIFICATION

PARAME	TER		Symbol	min	typ	max	Unit	Note
Ambient Temperature	1		Ta	20	25	30	°C	Logal High Corrent
Programming Vcc			Vcc	4.75	5.0	5.25	v	Sestad sol signi
Programming Pulse					Amus.	201 20		Sharlot thor today.
Amplitude			I.w	88	90	92	mA	Output Lookage Curven
Clamp Voltage			Vw	19.0	19.5	20.0	V	Couput Loriona Current
Ramp Rate				10	-	70	V/µs	
Pulse Width			t pw	7.1	7.5	7.9	μs	9V point/200Ω load
Duty Cycle			bnuis	70	tts Eliker Co	e - Inco	%	Paner Supply Current
Sense Current	+	1.1			Ams-	NA AN		Owing Hagle Voltage"
Amplitude			Is	19	20	21	mA	
Sense Voltage			Vs	7.4	7.5	7.6	V	Outpot Short Circuit Ci
Clamp Voltage				19.0	19.5	20.0	V	Note: Applicable to HSC 114
Ramp Rate				70	-	-	V/µs	
Address Setup Time			tsA	10	Ven.c_01	1. p. 504	μs	STORMAND DAM
Address Hold Time			t HA	10	Dot -	Today	μs	Diamentonian
Sense Setup Time			tss	0.7	-		μs	
Sense Hold Time	-04		t H S	0.7	-	_ 33	μs	Address Access Line
Additional Programming	g Pulse			1	1	1	time	Chip Enable Access Tin
Programming Pulse Nu	mber pe	r bit	n	_	-	10000	time	Chip Eashie Duable Tin



Quadruple TTL-to-MOS Clock Drivers

The HD2912, a clock driver for the MOS memory, has basically the NAMD function. Its input is a TTL level and its output becomes and NAMD function. Its input is a TTL level and its output becomes $V_{\rm CC}$ N MOS clock input level. It operates on two power supplies — $V_{\rm CC}$ (5V) and $V_{\rm DO}$ (12V). It entidopase taking as its load a maximum of ten units of 4K-bit N MOS memories and can drive a load capacity of 4DQ pF at high speed.

- tinosis ramerons leval 20M- LTT &
 - Switching time: 50 ns (max.)
- Note appoint drivable: 600pf
 - Mounted with 4 circuits
- Applicable tempe saure: 0 to 70°C



BPIN ARRANGEMENT

MARSOLUTE NAXMUM RATINGS

	* _{or} V	
Tig	**,3	

MEMORY SUPPORT CIRCUITS

BRECOMMENDED OPERATING CONDITIONS

csi			
Supply Voltage		7.1	

(Top View)

		wW -				
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$					
Input Corregt		· int				
					100	

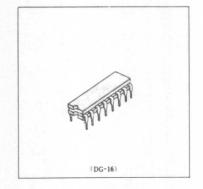
Formal Parellay

HD2912

Quadruple TTL-to-MOS Clock Drivers

The HD2912, a clock driver for the MOS memory, has basically the NAND function. Its input is a TTL level and its output becomes and N MOS clock input level. It operates on two power supplies — V_{CC} (5V) and V_{DD} (12V). It anticipates taking as its load a maximum of ten units of 4K-bit N MOS memories and can drive a load capacity of 400 pF at high speed.

- TTL-MOS level converter circuit
- Switching time: 50 ns (max.)
- Load capacity drivable: 600pF
- Mounted with 4 circuits
- Applicable temperature: 0 to 70°C



■ ABSOLUTE MAXIMUM RATINGS

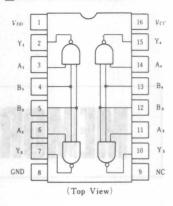
Item	Symbol	HD2912	Unit
0 1 17 1.	Vcc*	7.0	V
Supply Voltage	V _{DD} *	18.0	V
Input Voltage	Vin *	5.5	V
Load Capacitance	C L **	600	pF
Power Dissipation	P_T ***	800	mW
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tota	-65 to +150	°C

- * With respect GND
- * * per circuit * * * per package

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
C 1 V1.	Vcc	4.75	5.0	5.25	V
Supply Voltage	V_{DD}	11.4	12	12.6	V
Operating Temperature	Topr	0	25	70	°C
Load Capacitance	C _L	100	-	600	pF
Damping Resistance	R _D	10	-	-	Ω

■ PIN ARRANGEMENT



ELECTRICAL CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V$ $\pm 5\%$, $V_{DD}=12V$ $\pm 5\%$)

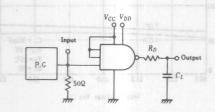
Item		Symbol	Test Condition	min	typ*	max	Unit
Input Voltage		VIL		2.0	_	-	V
Input voltage		VIH		_		0.8	V
Outrot Valence		Vol	$V_{in} = 2 \text{ V}, I_{OL} = 0.1 \text{ mA}$		0.45	0.6	V
Output Voltage		Von	$V_{in} = 0.8 \text{V}, I_{OH} = -0.1 \text{mA}$	$V_{DD} = 0.9$	11.5	-	V
	A	IIL	V ₁₂ =0.4V	_	-1	-1.6	mA
Input Current	В	IIL	7 V in = 0.4 V	_	-2	-3.2	mA
	A	IIH	77 0 437	_	_	40	μΑ
	В	IIH	$V_{in} = 2.4 \text{V}$	_		80	μΑ
		I_I	V., = 5.5V	_	_	1	mA
		IDDH	V = 0 V	_	16	24	mA
Power Supply Current		IDDL	V., = 5 V	_	_	0.5	mA
		Іссн	$V_{in} = 0 \text{ V}$	_	12	18	mA
		IccL	$V_{in} = 5 \text{ V}$		67	100	mA
Input Clamp Voltage		Vi	$I_{\rm in} = -12\mathrm{mA}$			-1.5	V

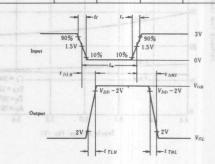
^{*} Vcc-5V, VDD-12V

SWITCHING CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V, VDD=12V)

Item	Symbol	Test Condition	min	typ	max	Unit
Rising Delay Time	t DLH		-	35	50	ns
Falling Delay Time	t DHL	C _L =300pF		25	45	ns
Rise Time	t TLH	$R_D = 0\Omega$		12	25	ns
Fall Time	t THL			12	25	ns

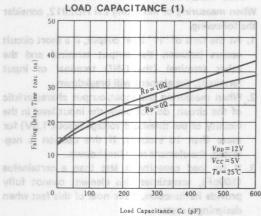
• TEST CIRCUIT AND WAVEFORMS





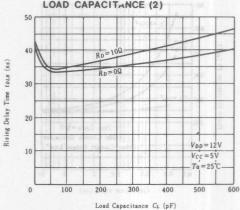
 $t_w = 250 \text{ns}, t_{cBcLe} = 350 \text{ns}, t_f = t_r = 10 \pm 1 \text{ns}$

FALLING DELAY TIME VS. COM SHIT

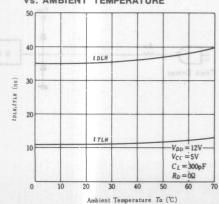


RISING DELAY TIME vs.

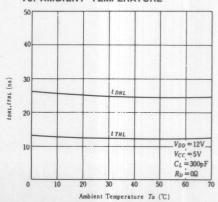
LOAD CAPACITANCE (2)



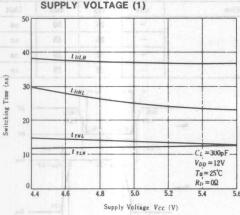
RISE TIME AND RISING DELAY TIME
vs. AMBIENT TEMPERATURE



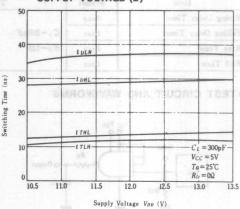
FALL TIME AND FALLING DELAY TIME vs. AMBIENT TEMPERATURE



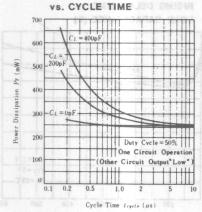




SWITCHING TIME vs. William War and SWITCHING TIME vs. DEMHATIME SUPPLY VOLTAGE (2)



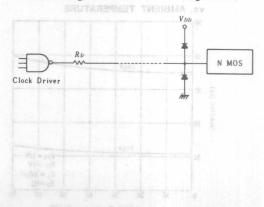
POWER DISSIPATION



ITEMS REQUIRING CARE WHEN USING THE HD2912 MIT YAJED DIGITAR

When measuring or mounting the HD2912, consider the following.

- 1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
- 2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.
- 3. If its load capacity is less than a certainalue (100pF), sometimes this element cannot fully provide its function. Take note of this fact when designing a system.
- 4. When mounting this element, it is recommended providing the output terminal with a damping resistor (RD) or a diode terminating circuit.



HD2916

Quadruple TTL-to-NMOS Clock Drivers

The HD2916, a clock driver for the MOS memory, basically possesses a NAND function. Its Input is a TTL level and its output becomes N MOS clock input level. It operates on two power supplies — V_{CC} (5V) and V_{DD} (12V). Assuming that a maximum of five units of 4K-bit N MOS memories may be connected, it is designed to drive a load capacity of 200pF at high speeds.

■ FEATURES • TTL-MOS level converter

Average power consumption: 600mW (max.)

Load capacity drivable: 300pF

Switching time: 50 ns (max.)

Mounted with 4 circuits
 Applicable temperature: 10 to 65°C

■ ABSOLUTE MAXIMUM RATINGS

Item TARAMA	Symbol	HD2916	Unit
	Vcc*	-0.5 to +7	V
Supply Voltage	V _{DD} *	-0.5 to +15	V
Input Terminal Voltage	V _{IN} *	-0.5 to $+5.5$	V
Output Load Capacitance	C L **	300	pF
Power Dissipation	P_T ***	700	mW
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tate	-50 to +150	°C

* With respect to GND

* * Per circuit * * * Per package

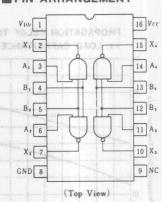
■ RECOMMENDED OPERATING CONDITION

of tem	Symbol	min	typ	max	Unit
Complex Voltage	Vcc	4.75	5.0	5.25	V
Supply Voltage	V_{DD}	11.4	12.0	12.6	V
Operating Temperature	Topr	10	25	55	°C
PELAY TIME	VIH	2.0	-	5.5	V
Input Voltage Level	VIL	-0.5	_	0.8	V

ENGLES WAVEFORE TEST

(DG-16A)

PIN ARRANGEMENT



ELECTRICAL CHARACTERISTICS (Ta=10 to 55°C, $V_{cc}=5V$ $\pm 5\%$, $V_{DD}=12V$ $\pm 5\%$)

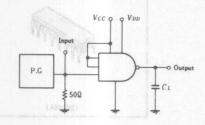
Item		Symbol	Test Condition	min	typ*	max	Unit
		IIH	$V_{IN} = 2.4 \text{V}$	-	-	40	μΑ
	A	IIL	$V_{IN} = 0.4 \text{V}$		-1	-2	mA
Input Current	В	IIH	$V_{IN}=2.4 \text{ V}$	<u>18</u> 1		80	μΑ
	В	IIL	$V_{IN}=0.4V$	-	-2	-4	mA
		Von	$V_{IN} = 0.8 \text{V}, I_{OH} = -50 \mu \text{A}$	$V_{DD} - 0.7$	$V_{DD} - 0.4$	-	V
Output Voltage		Vol	$V_{IN} = 2.0 \text{V}, I_{OL} = 50 \mu \text{A}$	-	0.3	0.45	V
To-East		IDDH	V _{IN} = 0 V		13	20	mA
S 1 C		Іссн	$V_{IN} = 0 \text{ V}$		13	40	mA
Supply Current		IDDL	$V_{IN} = 5 \text{ V}$	-		39	mA
111.5 12.0 12.5 13.0		Of Iccs 201	V _{IN} =5V 88 88	0.1	40	60	mA
Average Power Dissipation		Ртл	C_L =300pF, f =1MHz t_W =0.5 μ s, one circuit operation	Vertage Van	300	600	mW

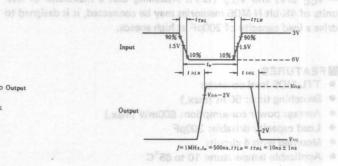
^{*} Vcc=5V, VDD=12V

SWITCHING CHARACTERISTICS (Ta=10 to 55°C, $V_{cc}=5V$ $\pm 5\%$, $V_{DD}=12V$ $\pm 5\%$)

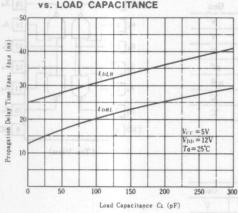
Item	Symbol	Test Condition	min	typ	max	Unit
	t DLH	C _L -200pF	driver	elack	50	ns
Output Delay Time	toHL	$f = 1 \text{MHz}$ $t_W = 0.5 \mu \text{s}$	ar en ,m Jevel tra	morner u mi Annin	50	ns

• TEST CIRCUIT & WAVEFORMS

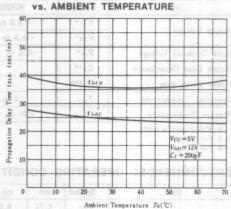




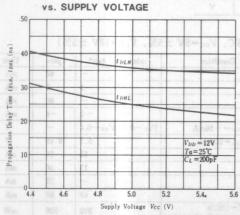
PROPAGATION DELAY TIME vs. LOAD CAPACITANCE



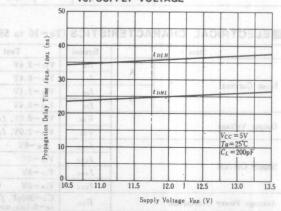
PROPAGATION DELAY TIME

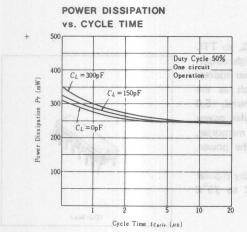


PROPAGATION DELAY TIME



PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE





■ITEMS REQUIRING CARE WHEN USING THE HD2916

When measuring or mounting the HD2916, consider the following:

- At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
- 2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.

· Pin Compatibility MC10125 or HD10126

HD2923

Quadruple ECL to TTL Drivers

BITEMS REQUIRING TARE WHEN USING

The HD2923 is a monolithic, high speed Quadruple ECL to TTL Driver which accepts ECL input signals. It provides high output current suitable for driving the TTL clock inputs or other address multiplexing inputs of N-channel MOS memories such as the HM4816A of MK4116. Power supply requirements are ground, +5.0 Volts and -5.2 Volts. The HD2923 requires no particular power supply sequencing in order to assure standby mode of memories, because the outputs are always "high" at applying the power. Propagation delay is 10ns MAX.

The HD2923 is fabricated by means of HITACHI's Schottky Bipolar technology to assure high performance over the 0°C to 75°C ambient temperature range.

FEATURES

- High Speed t_{pd} = 10ns MAX. (50% to 2.2V dc out or to +1.0V dc out, 200pF Load)
- 10K ECL Compatible Inputs
- Pin Compatibility MC10125 or HD10125

■ ABSOLUTE MAXIMUM RATINGS

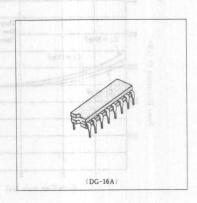
Symbol	Value	Unit
Vcc	-0.5 to +7	V
V_{EE}	-7 to +0.5	V
Vin	V _{EE} to +0.5	V
Vout	-1.0 to Vcc+1	V
P_T	1.0	W
T_{opr}	-10 to +85	°C
Tota	-65 to +150	°C
	Vcc VEE Vin Vout PT Topr	V_{CC} $-0.5 \text{ to } +7$ V_{EE} $-7 \text{ to } +0.5$ V_{in} $V_{EE} \text{ to } +0.5$ V_{out} $-1.0 \text{ to } V_{CC}+1$ P_T 1.0 T_{opr} $-10 \text{ to } +85$

^{*} under bias

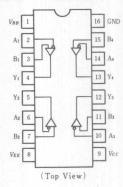
RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
	V_{EE}	-5.46	-5.2	-4.94	V
Input Voltage	V_{IH}	-1.025	-	-	V
	V_{IL}	-	-	-1.520	V
Operating Temperature	Topr	0	_	75	°C

POWER DISSIPATION



PIN ARRANGEMENT



The V_{BB} reference voltage is available on pin 1 for use in single ended input biasing

TRUTH TABLE

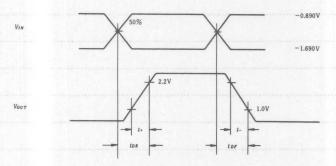
Input		Output	
A	В	Y	
Н	V_{BB}	L	
L	V_{BB}	Н	
Н	L	L	
L	Н	Н	
V_{BB}	Н	Н	
V_{BB}	L	L	
Open	Open	Н	

■DC CHARACTERISTICS

Item	Symbol	Test Condition	min	typ	max	Unit
Power Supply Drain Current	$-I_{EE}$	$V_{\mathcal{E}\mathcal{E}} = -5.2 \text{V}, \ V_{\text{CC}} = 5.0 \text{V}$	_	22	27	mA
	Іссн			23.5	29	mA
	IccL		-	34.5	42	mA
Input Current	I in H	$V_{IN} = -0.81 \text{V}$			115	μΑ
Input Leakage Current	Ісво	$V_{IN} = -5.2 \text{V}$	-	_	1.0	μ A
Output Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.7		-	V
	Vol	IoL=5.0mA			0.5	V
Threshold Voltage	VOHA	$V_{IH} = -1.1 \text{V}, I_{OH} = -1.0 \text{mA}$	2.7		-	V
	VOLA	$V_{IL} = -1.48 \text{V}, I_{OL} = 5.0 \text{mA}$	-	-	0.5	V
Indeterminate Input Protection Tests	Vons	All inputs = V_{EE}	2.7			v
		All inputs = Open	2.7	-	_	
Reference Voltage	V_{BB}		-1.420	7 FEV. 10 <u>11</u> 4 F.	-1.150	V
Common Mode Rejection Tests	V онс	$V_{INH} = 0.300 \text{ V}, \ V_{INL} = -0.825 \text{ V}$	2.7	-	-	v
		$V_{INH} = -1.890 \text{V}, \ V_{INL} = -2.890 \text{V}$	2.7	-	_	V
	Volc	$V_{INH} = 0.300 \text{V}, V_{INL} = -0.825 \text{V}$		· · · · · ·	0.5	V
		$V_{INH} = -1.890 \text{ V}, \ V_{INL} = -2.890 \text{ V}$	-	-	0.5	

MAC CHARACTERISTICS

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t DR	50% to +2.2V, C _L =200pF	-	_	10	ns
	tor	50% to +1.0V, C _L =200pF		_	10	ns
Rise Time	t +	+1.0V to +2.2V, C _L =200pF		lene—	5	ns
Fall Time	t-	+2.2V to +1.0V, C _L =200pF		-	5	ns



MEMO nepat Leakage Correger | Fara | Flare 5.2V - - 2.0 MA

